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ANNUAL ARMENIAN MICROELECTRONICS OLYMPIAD TESTS AND PROBLEMS

Yerevan - 2009

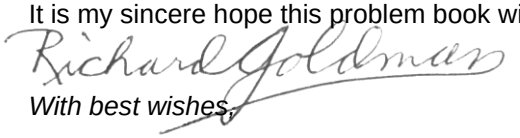
Welcome!

The problem book that you hold in your hands is the latest contribution of Armenia to the advancement of microelectronics. I am sure you will find it very modern, and useful. This is the book of tests and problems of the Annual Armenian Microelectronics Olympiad. At the same time, it will also be a very valuable resource for students, Masters and PhDs of microelectronics and similar engineering disciplines, providing them an opportunity to assess and improve their knowledge, as well as to develop solution skills of tests and problems.

The results of the First to the Fourth Olympiad witnessed that the book has served its purpose and has become “a table book” for participants.

As the third problem book of tests and problems focused on the development of Armenia's IT sector, it is a unique contribution in the key area of training highly qualified specialists. It will also contribute to the realization of the goals of the next Annual Armenian Microelectronics Olympiads, contributing to the ascension of Armenian microelectronics to a state-of-the-art and leading branch of industry.

It is my sincere hope this problem book will take its notable place in your professional library.



With best wishes,

Rich Goldman,

Vice president for Corporate Marketing of Synopsys Inc.,

CEO of Synopsys Armenia CJSC,

President of Armenian Microelectronics Olympiad Organizing Committee,

Honorable Doctor of SEUA

PREFACE

During the last three years the First (September 22-25, 2006), the Second (September 18-25, 2007), the Third (September 16-29, 2008) and the Fourth (September 15-30, 2009) Armenian Microelectronics Olympiads took place (http://www.microolymp.am). The goals of organizing the Armenian Microelectronics Olympiad were to: stimulate the further development of microelectronics in Armenia, discover young, talented resources (University students and specialists of microelectronics area companies up to 30 years), increase interest towards microelectronics among them, understand the level of knowledge in the field of microelectronics among young specialists to make necessary adjustments to educational programs in the future. Considering the successful experience of holding the Armenian Microelectronics Olympiads, it has become continuous, annual. It is not excluded that the Olympiad becomes international in the coming years. The success of the previous Olympiads was mainly conditioned by the finance assistance and huge organizational efforts of its main sponsor SYNOPSYS ARMENIA CJSC (CEO Rich Goldman, General Manager Hovik Musayelyan) and sponsors VIVACELL-MTS/K-Telekom CJSC (General Manager Ralph Yirikyan), USAID CAPS project (coordinator of IT cluster Armen Abrahamyan), Enterprise Incubator Foundation (director Bagrat Yengibanryan), ACBA bank (president Stepan Gishyan), Unicomp CJSC (director Armen Baldryan), Microsoft RA LTD (General Manager Grigor Barseghyan), Arminco CJSC (General Manager Andranik Aleksanyan), Virage Logic International Corporation (Executive Director Varuzhan Meserejyan), Union of Manufacturers & Businessmen of Armenia (UMBA) (Executive President Arsen Ghazaryan), Viasphere Technopark CJSC (General Manager Aram Vardanyan), Apaven Ltd (Director Gagik Makaryan), Union of Information Technology Enterprises (UITE) (Executive Director Karen Vardanyan), web-site developer “N-Sourcer” TM “Art Site” (Director Areg Harutyunyan), Yerkir Media TV Company (Director of media and political part Gegham Manukyan), ARKA Agency (Director Konstantin Petrosov), Mediastyle LTD (General Manager Vardan Asatryan), Ekonomika Magazine (Editor-in-Chief Lyusya Mehrabyan), “Delovoy Express” Weekly (Editor-in-Chief Eduard Naghdalyan), “168 Hours” Daily (Editor-in-Chief Satenik Seyranyan). In the sense of providing participants great assistance has been demonstrated by universities: SEUA (rector Vostanik Marukhyan, pro-rector Ruben Aghgashyan), YSU (rector Aram Simonyan, pro-rector Aleksandr Grigoryan), Russian-Armenian (Slavonic) State University (rector Armen Darbinyan, pro-rector Gagik Sargsyan), as well as Heads of Companies: SYNOPSYS ARMENIA CJSC (CEO Rich Goldman, General Manager Hovik Musayelyan), Instigate Inc. (Director Vahagn Sargsyan) as well as Gyumri Information Technologies Center (Executive Director Jason Kazarian). The first stage of the Olympiad was at the same time held in Gyumri for the first time. I express my deep gratitude to the mentioned people as well as the rest of the members of Organizing Committee of the Armenian Microelectronics Olympiads – Andranik Hovhannisyan (Deputy General Manager of SYNOPSYS ARMENIA CJSC), Vladimir Harutyunyan (Head of YSU microelectronics Chair), Harutyun Terzyan (SEUA Professor), Eduard Ghazaryan (Head of department of Russian-Armenian (Slavonic) State University), Andranik Aleksanyan (General Manager of Arminco CJSC), members of Program Committee Valeri Vardanyan (Scientific Worker of Virage Logic Corporation), David Parent (Associate Professor of San-Jose State University (USA, CA)), Slavik Melkonyan (YSU Professor), Artur Minasyan (Senior Engineer in SONICS ARMENIA HOLDINGS Armenian Design Center), as well as Gayane Markosyan who illustrated the event (SEUA Associate Professor, Senior Coordinator of SYNOPSYS ARMENIA CJSC Educational Department).

The Olympiads were held giving the participants a test with easy questions (the first stage) and problems requiring peculiar solutions (the second stage). Test questions and problems together with their solutions set in the from I-IV Armenian Annual Microelectronics Olympiads are included in the book. Test questions and problems are related to VLSI Design and EDA areas. They are classified according to the basic sections of the above mentioned areas.

1. Digital integrated circuits
2. Analog integrated circuits
3. RF integrated circuits
4. Semiconductor physics and electronic devices
5. Semiconductor technology
6. Numerical methods and optimization
7. Discrete mathematics and theory of combinations
8. Object-oriented programming

The problem book, first of all, is anticipated for the future participants of the Armenian Microelectronics Olympiad of the coming years. In my opinion, it will contribute to the increase of knowledge level of Olympiad participants. At the same time, it can also be useful for other students, Masters, PhDs and engineers of the above mentioned areas.

The problem book also contains to some extent similar test questions and problems as they have been included in different, equivalent variants during the Olympiads.

The problem book, in its future publications, will be filled with the test questions and problems of the coming Olympiads.

You can send your remarks at microelectronics_olympiad@synopsys.com.

I express my deep gratitude to the below mentioned authors of the problem book most of whom are also members of Olympiad Program Committee.

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- Slavik Melkonyan – YSU Professor, Sci.D.
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whom I also express my deep gratitude.

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Honorable Scientist of Armenia,
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TESTS AND PROBLEMS

1. DIGITAL INTEGRATED CIRCUITS

a) Test questions

1a1. There is tri-state buffer, in which internal delays can be ignored. Right after z state is set, the output voltage level will be:

A. VDD/2, where VDD is supply voltage
B. High or low, depending on the state before z state is set
C. Indefinite
D. High
E. Low

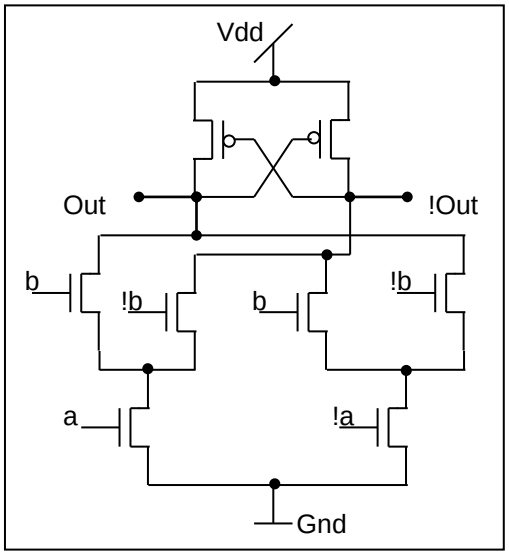
1a2. In CMOS ICs, p - MOS transistor is usually configured as:

A. No potential is given to substrate
B. Substrate is connected to source
C. *Substrate is connected to drain*
D. The highest potential is given to substrate
E. The lowest potential is given to substrate

1a3. There is JK flip-flop. Mark the prohibited input combination

A. J=1, K=1
B. J=1, K=0
C. J=0, K=1
D. J=0, K=0
E. No prohibited combination

1a4. What logic function is implemented by the shown circuit?



A. AND
B. XOR-XNOR
C. AND-NAND
D. OR-NOR
E. MUX-MUXI

1a5. Which is the Canonical Disjunctive Normal Form (CDNF) of the function described by the following truth table?

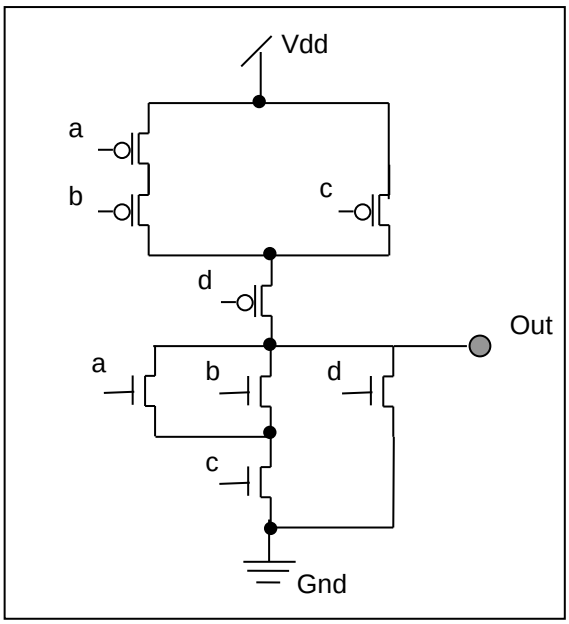
Inputs			Output
a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

A. y=!a&b&!c+!a&b&c+a&b&!c+a&b&c
B. y=!a&!b&!c+!a&!b&c+a&!b&!c+a&!b&c
C. y=(a+b+c)&(a+b+!c)&(!a+b+c)&(!a+b+!c)
D. y=(!a+!b+!c)&(!a+!b+c)&(a+!b+!c)&(a+!b+c)
E. y=(a+!b+c)&(a+!b+!c)&(!a+!b+c)&(!a+!b+!c)

1a6. Threshold voltage of MOS transistor is called the voltage w*hich is necessary to be applied between the gate and the source:*

A. For 1uA current flow through drain
B. Of the transistor for current flow through drain which is 10 times more then leakage current of transistor
C. Of the transistor for average concentration of charge carriers that maintain transistor's conductance be equal to average concentration of majority charge carriers in substrate in channel formation place
D. Of the transistor for average concentration of charge carriers that maintain transistor's conductance be equal to average concentration of minority charge carriers in substrate in channel formation place
E. Of the transistor for the transistor to be saturated

1a7. What formula describes the circuit?



A. Out = !((!a+!b)&!c+!d)
B. Out = !((a+b)&c+d)
C. Out = !((a&b+c)&d)
D. Out = ((!a+!b)&!c+!d)
E. Out = !((!a&!b+!c)&!d)

1a8. Which statement is correct?

A. Charge-coupled devices' (CCD) work is based on processes occurring in bipolar transistors
B. CCD's frequency internal limit is influenced by thermo generation of charge carriers
C. CCD's frequency parameters do not depend on the degree of semiconductor's surface energetic levels
D. CCD's frequency properties do not depend on the type of semiconductor
E. CCDs are static devices

1a9. Which of the shown answers more contributes to the successful solution of cells' placing problem?

A. Maximum distance between high frequency circuits
B. Maximum distance between low frequency circuits
C. Maximum proximity of more related cells
D. A. and C. together
E. B. and C. together

1a10. One of the rules of concurrent modeling is

A. Lc(γ) list defined for an external output line composes the set of testable faults which can be found by the given input set (vector)
B. Single stuck-at fault (SSF) model assume that there is only one fault in tested logic circuit
C. Two types of stuck-at logic faults - stuck-at-1 fault (SA1 or s@1) and stuck-at-0 fault (SA0 or s@0)
D. Lc(γ) list defined for an external output line composes the set of testable faults which can be found by an output set (vector)
E. None

1a11. In state-of-the-art integrated circuits the minimum width of interconnect's transmission lines is limited by
- *A. Resolution of the lithography process*
- *B. Mutual agreement of customer and manufacturer*
- *C. The desire of designer*
- *D. Technological method to get thin layers*
- *E. The phenomena of electromigration*

1a12. The increase of the logic circuit organization's parallelism mostly leads to
- *A. The increase of performance*
- *B. The increase of the number of primary outputs*
- *C. The decrease of the number of logic cells*
- *D. A. and B. together*
- *E. B. and C. together*

1a13. The $f(x_1, x_2, x_3)$ function accepts 1 value on 0, 3, 5, 6 combinations. What class does the given function belong to?
- *A. Constant 0*
- *B. Constant 1*
- *C. Linear and dual*
- *D. Dual*
- *E. Monotone*

1a14. Operation of Gunn diode is based on
- *A. The effect of semiconductor inversion in strong electrical field*
- *B. The appearance of negative differential impedance in strong electrical field*
- *C. The tunnel effect in strong electric field*
- *D. The rectifying properties of p-n junction*
- *E. The contact effects between metal and semiconductor*

1a15. Which of the shown answers more contributes to the increase of the fan-out?
- *A. Increase of cells' input resistance*
- *B. Increase of cells' output resistance*
- *C. Decrease of cells' output resistance*
- *D. A. and B. together*
- *E. A. and C. together*

1a16. Which of the following statements is wrong for synchronous FSM?
- *A. Memory element competition, static and dynamic risks in combinational circuits are dangerous*
- *B. The abstract presentation of the automaton is used for building circuit*
- *C. Required synchronization of asynchronous input signals with clock signals*
- *D. All FFs trigger at the same clock signal*
- *E. The wrong answer is missing*

1a17. The common emitter configuration compared with common base configuration
- *A. Increases frequency properties*
- *B. Increases the collector junction's resistance*
- *C. Increases collector junction's breakdown voltage*
- *D. Increases the current gain*
- *E. Decreases the thermal component of collector current*

1a18. Which of following methods of interconnect designing more contributes to speed increase?
- *A. Increase of interconnect layers*
- *B. Decrease of total length of interconnects*
- *C. Decrease of length of signal processing critical path*
- *D. B. and C. together*
- *E. A. and C. together*

1a19. Among the following principles, which is wrong for concurrent simulation?
- *A. Classification of vectors according to quality, move low quality vectors in the beginning of simulation, elimination of detected faults – it increases simulation speed, reduces simulation time*

B. *Any subset of faults is simulated, extrapolation of fault coverage is executed according to obtained results*
C. *IC simulation, estimation of vectors' quality - 01 or 10 toggle node number, toggle coverage*
D. *For the given vector there is strict correlation between detectable fault number and 01, 10 toggle number*
E. *None*

1a20. There is an inverter which has a passive capacitive load. If supply voltage increases,
A. Rise will increase, Fall will decrease
B. Fall will increase, Rise will decrease
C. Output transition time will decrease
D. Output transition time will increase, as during switching the load must be charged by larger □U voltage
E. Output transition time will remain the same, as □U will increase, but charging current will also increase

1a21. The transfer characteristic of MOS transistor is *the dependence of:*
A. Drain voltage on gate-source voltage
B. Drain voltage on drain-source voltage
C. Drain current on drain-source voltage
D. Drain current on gate-source voltage
E. Gate current on gate-source voltage

1a22. Latch - up phenomena is proper to
A. ECL circuits
B. Only CMOS circuits
C. N-MOS and CMOS circuits
D. P-MOS and CMOS circuits
E. All bipolar circuits

1a23. Which one is prohibited input combination for RS latch?
A . R=0, S=1
B. R=1, S=0
C. R=0, S=0
D. R=1, S=1
E. There is no prohibited combination

1a24. Define in which state will Johnson's 6 bit counter go, after the 10^{th} pulse is applied. Initial state is 000111.
A. 011110,
B. 001011,
C. 101010,
D. 011010,
E. The correct answer is missing

1a25. How many pins does the bipolar transistor have?
A. 1- emitter,
B. 2- emitter and base,
C. 2- base and collector,
D. 2- emitter and collector;
E. 3- emitter, base and collector,

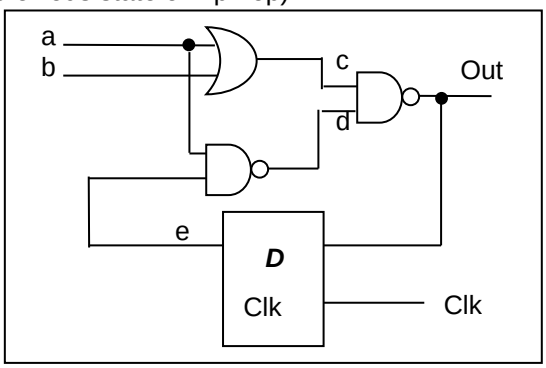
1a26. What semiconductor material is mostly used in integrated circuits?
A. Ge
B. Si
C. GaAs
D. Fe
E. Zn

1a27. From the following statements which is wrong for DRAM?
A. Usually one MOS transistor is used to keep 1 bit in memory
B. FF is as a memory cell
C. Address inputs are multiplexed

D. DRAMs are considered energy dependent
E. The wrong answer is missing

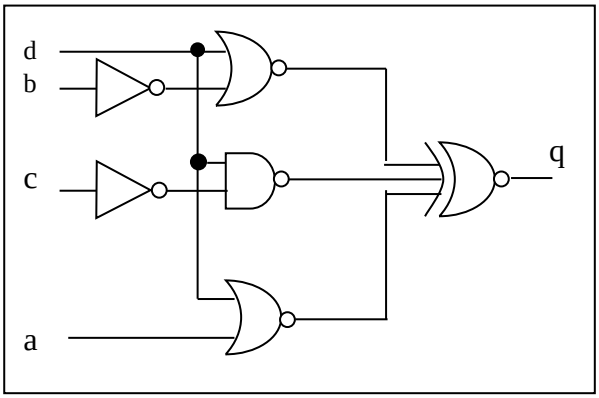
1a28. In logic design level the following is designed:
A. Stand alone device which is divided up to such multibit blocks as registers, counters, etc
B. Stand alone logic gate or FF, which consists of electronic components – transistors, diodes, etc
C. Stand alone semiconductor component, e.g. transistor
D. Digital device the components of which are separate logic gates and FFs
E. General system which consists of RAM memory device, datapath devices, etc

1a29. Identify the synchronous model of the following circuit. (TP- delays, TF-transition time, "p"-previous state of flip-flop).



A. c=a & b,
d=!(a | e),
Out=!(c & d),
e=posedge(Clk ? Out: 'p'), TP=0.1n,
B. c=a | b
d=!(a | e),
Out=!(c & d),
e=posedge(Clk) ? Out: 'p'
C. c=a & b,
b=!(a | e),
Out=!(c & d),
e=!(posedge(Clk)? Out: 'p'), TF=0.1n
D. c=a & b, TP=0.1n,
d=!(a | e), TP=0.1n,
Out=!(c & d), TP=0.1n,
e=posedge(Clk) ? Out: 'p', TP=0.1n,
E. c=a & b, TP=0.1n,
d=a | e, TP=0.1n,
Out=c & d, TP=0.1n,
e=!(posedge(Clk)? Out: 'p'), TP=0.1n,

1a30. In case of which switching the occurrence of dynamic fail risk is possible in the following circuit?



A. a=0-1,	*b=1,*	*c=0,*	*d=1*
B. a=0,	*b=0-1,*	*c=0,*	*d=0*
C. a=0,	*b=1,*	*c=0,*	*d=0-1*

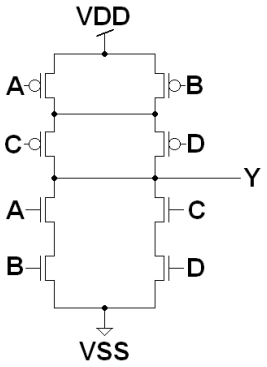
D. a=1, b=0, c=1, d=0-1
E. a=0-1, b=0, c=1, d=0

1a31. In component level of the design the following is being designed:
A. A separate semiconductor device, e.g. transistor
B. A separate device, which is being disassembled until diverse components, such as registers, calculators, etc
C. A separate logic gate or FF which consists of electronic components – transistors, diodes, etc
D. A general system which consists of operative memory device, numerical device, etc
E. A digital device which consists of separate logic gates and FFs

1a32. In order to prevent latch-up in CMOS circuits it is necessary
A. To increase the parasitic capacitances between the buses of output buffer's parasitic bipolar transistors
B. To increase the gain of parasitic bipolar transistors
C. Put the drains of n and p transistors as close as possible
D. Put n+ guard ring around n+ source/drain
E. Put p+ guard ring around n+ source/drain and put n+ guard ring around p+ source/drain

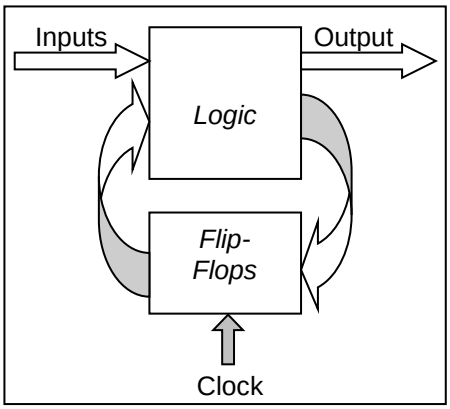
1a33. In digital circuits p-MOS transistor's
A. Delays do not depend on the supply voltage
B. Threshold voltage is proportional to the delay of transistor
C. Delays do not depend on temperature
D. The highest potential is usually applied to substrate
E. Dynamic power dissipation depends only on transistor resistance

1a34. For the following circuit mention the input which will have the maximum input-to-output delay.



A. A
B. C
C. D
D. B
E. All are equal

1a35. In the following digital system, where setup time of FF is T_{SU}, delay T_{CLKQ}, and delay of logic part T_{LOGIC}, the highest clock frequency will be



A. $f=1 / T_{LOGIC}$
B. $f=1 / (T_{LOGIC}+T_{SU})$
C. $f=1 / (T_{LOGIC}+T_{CLKQ}+T_{SU})$
D. $f= T_{LOGIC}+T_{CLKQ}+T_{SU}$
E. $f=1 / (T_{LOGIC}+2*T_{CLKQ}+T_{SU})$

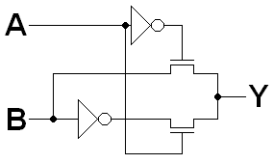
1a36. Which is the sum of the following two signed hexadecimal numbers if the addition is performed by saturation adder: 81H + FEH?
A. 7FH
B. FFH
C. 00H
D. 80H

E. 77H

1a37. Which of the following is the binary representation of 3.25 decimal number in 4bit, 4bit fixed point format?

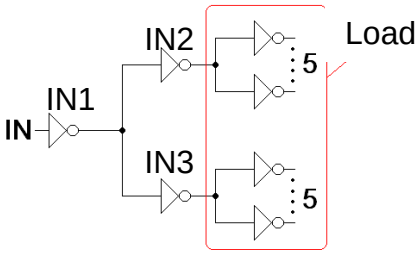
A. 01110101
B. 10001010
C. 00110100
D. 00111010
E. 01111001

1a38. XOR logic circuit is shown in the figure. Which is the disadvantage of the circuit?



A. Input capacitances are large
B. Delays are large
C. Output 1 level is degradated
D. Output 0 level is degradated
E. Power consumption is large

1a39. Buffer circuit composed by I1, I2, I3 identical inverters is shown in the figure. The I2 and I3 are loaded by 5 similar inverters. What expression is the average delay of the buffer defined by?



A. $(R_p + R_n)\cdot(2\cdot C_{out} + 7\cdot C_{in})$

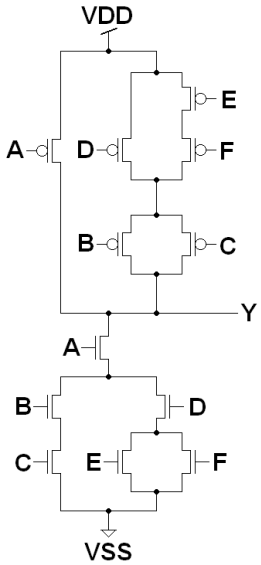
B. $(R_p + R_n)\cdot(5\cdot C_{out} + 7\cdot C_{in})$

C. $(R_p + R_n)\cdot(C_{out} + 7\cdot C_{in})$

D. $2\cdot(R_p + R_n)\cdot(2\cdot C_{out} + 7\cdot C_{in})$

E. $(R_p + R_n)\cdot(2\cdot C_{out} + 5\cdot C_{in})$

1a40. What logic function is realized in the shown circuit?



A. $A\cdot(B\cdot C + D\cdot(E+F))$

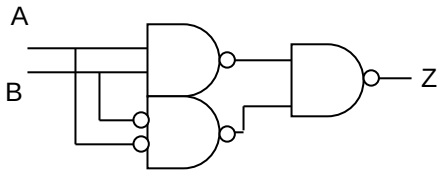
B. $A\cdot(B + C + D\cdot(E+F))$

C. $A + B\cdot C + D\cdot(E+F)$

D. $\overline{A\cdot(B\cdot C + D\cdot(E+F))}$

E. $\overline{A + B\cdot C + D\cdot(E+F)}$

1a41. What formula does the given circuit describe?



A. Z=A&B+(!A&!B)
B. Z=(!A&B)+(!B&A)
C. Z=!A&B
D. Z=A&(!B)
E. Z=A+!B

1a42. Saturation condition of NMOS transistor has the following view:

A. $V_{DS} \le V_{GS} - V_{THN}$

B. $V_{DS} \ge V_{GS} - V_{SB}$

C. $V_{GS} \ge V_{DS} - V_{THN}$

D. $V_{DS} \ge V_{GS} - V_{THN}$

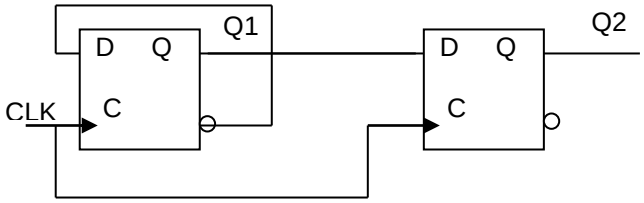
E. $V_{DS} \ge V_{GS} + V_{THN}$

1a43. Conjunctive Normal Form (CNF) of the function in the following truth table has the following view:

a	b	c	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

A. (!a+!b+!c)& (!a+b+c)& (!a+b+c)& (!a+!b+c)
B. (a+!b+!c)& (!a+b+c)& (!a+b+c)& (!a+!b+!c)
C. (!a+!b+c)& (!a+!b+c)& (!a+b+c)& (!a+!b+c)
D. (a+b+c)& (!a+b+c)& (!a+b+!c)& (!a+!b+c)
E. !a&!b&!c+ !a&b&!c+ a&!b&!c+ a&b&c

1a44. In what state will the below shown automaton go after applying four pulses if the initial state is Q1Q2=1x?



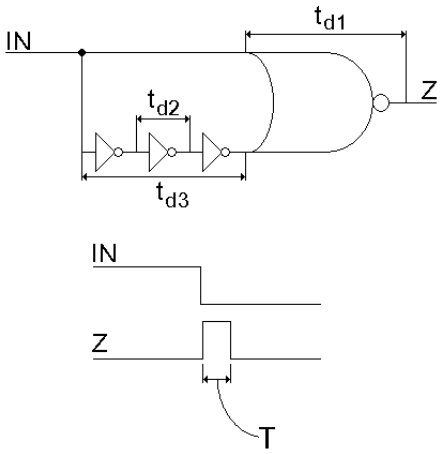
A. 01
B. 10
C. 00
D. 11
E. x1

1a45 In digital circuits, for an n-MOS transistor
A. The lowest potential is usually given to substrate

B. Delays do not depend on the supply voltage
C. Threshold voltage is proportional to the delay of transistor
D. Delays do not depend on temperature
E. Dynamic power dissipation depends only on transistor resistance

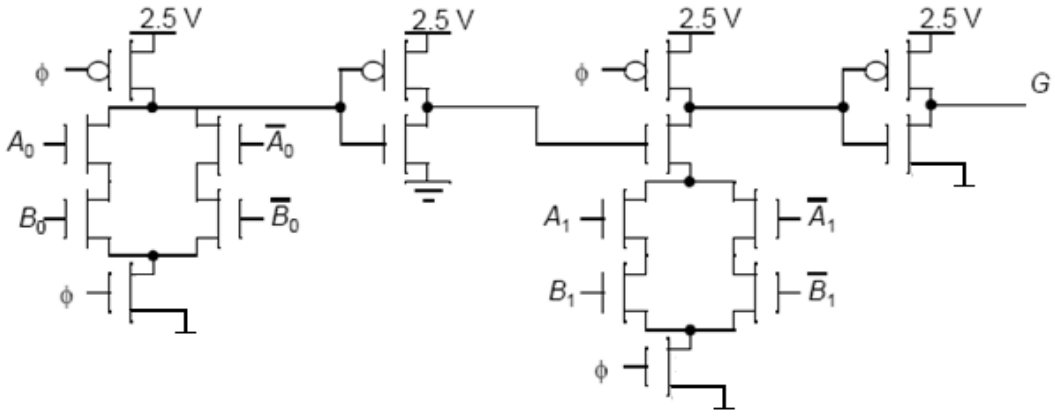
1a46. Which is the sum of the following two signed hexadecimal numbers if the addition is performed by saturation adder: 12H + 70H?
A. 7FH
B. FFH
C. 00H
D. 80H
E. 82H

1a47. T duration of the short pulse, obtained on the output of the given circuit, is mainly defined by?



A. td1
B. td3
C. td2
D. td1 + td2
E. td1 + td3
delays.

1a48. If A and B are interpreted as two-bit binary words, A = {A1, A0} and B = {B1, B0} then what interpretation can be applied to output G?



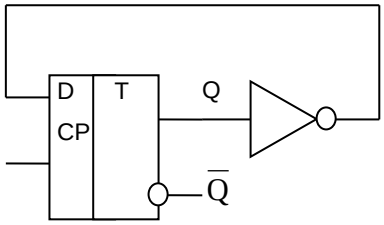
A. Scalar product: G=(A0&B0)+(A1&B1)
B. Modulo-2 sum: G=(A0⊕B0) ⊕ (A1⊕B1)
C. Equality: G=(A = = B)
D. Non-equality G=(A != B)
E. Logic sum G=A0+B0+A1+B1

1a49. Considering that NOR2 cell's inputs are independent and equally distributed, which is the probability of output switching?

A. 0.25
B. 0.375
C. 0.5
D. 0.75
E. 0.875

1a50. Assuming $k_n=2k_p$, in what case will the resistances from the output of NOR2 cell to VDD and VSS be equal?
A. $W_p=W_n$
B. $W_p=2W_n$
C. $W_p=4W_n$
D. $W_p=6W_n$
E. $W_p=8W_n$

1a51. The figure shows the circuit of frequency divider.

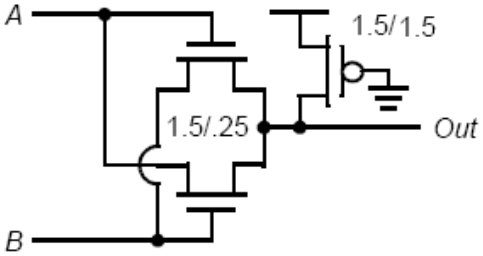


What expression gives the minimum period of clock pulses?
A. $T_{min}=t_{su}+t_{c2q}+t_{pinv}$
B. $T_{min}= t_{c2q}+t_{pinv}$
C. $T_{min}=t_{su}+t_{hd}+t_{c2q}+t_{pinv}$
D. $T_{min}= t_{hd}+t_{c2q}+t_{pinv}$
E. $T_{min}= t_{su}+t_{hd}+t_{pinv}$

1a52. How many digits does the thermometer code have which is obtained after modifying 4-bit binary code?
A. 16
B. 4
C. 15
D. 8
E. 32

1a53. For the same size inverter what version has minimum leakage current?
A. PMOS low-vt, NMOS high-vt
B. PMOS standard-vt, NMOS high-vt
C. PMOS high-vt, NMOS standard-vt
D. PMOS high-vt, NMOS low-vt
E. PMOS low-vt, NMOS standard-vt

1a54. What logic function does the circuit implement?



A.OUT=A+B
B.OUT=A&B
C.OUT=!A+!B
D.OUT=!A&!B
E.OUT=A⊕!B

1a55. Which is the basic consequence of MOS transistor's degradation due to warm carriers?
A. The increase of threshold voltage
B. The decrease of threshold voltage
C. The increase of channel resistance

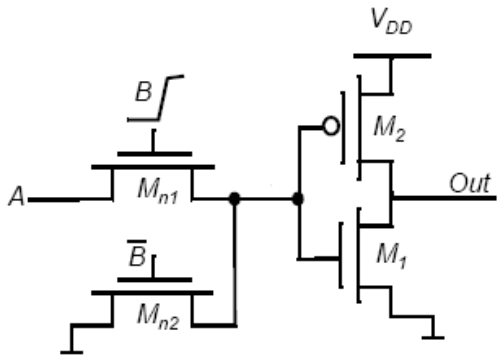
D. The decrease of channel resistance
E. The decrease of drain-package disruption voltage

1a56. Assuming $k_n=rk_p$, in what case will the resistances from the output of 3NAND cell to VDD and VSS be equal?
A. $W_p/W_n=r$
B. $W_p/W_n=r/9$
C $W_p/W_n=r/6$
D. $W_p/W_n=r/3$
E. $W_p/W_n=2r/3$

1a57. Which one of the given expressions is wrong?
A. A⊕!B = !A⊕B
B. 1⊕!B⊕A = B⊕A
C. A⊕B =! A⊕!B
D. A⊕!B = !A⊕!B
E. !A⊕B = !(A⊕B)

1a58. What is the minimum number of transistors in a pass gate implemented 1:4 multiplexer, assuming that normal and complemented select variables are available:
A. 16
B. 12
C. 8
D. 6
E. 4

1a59. What function does the circuit implement?



A. OUT=A+B
B. OUT=A&B
C. OUT=!A+!B
D. OUT=!A&!B
E. OUT=A⊕!B

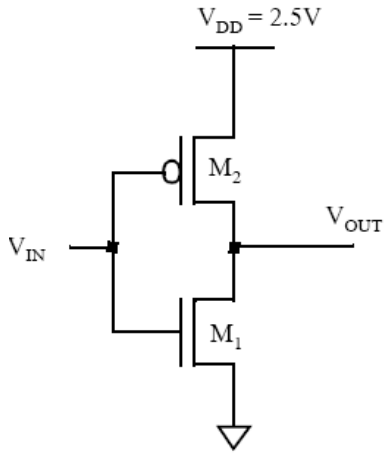
1a60. C capacitance is connected to the end of interconnect line with L length, line parameters are c [F/m], r [Ohm/m]. By what formula is the signal delay time in the line given?
A. 0.7rc
B. 0.7Lr(C+c)
C. 0.7Lr(C+Lc/2)
D. 0.7Lr(C+Lc)
E. 0.7Lr(C/2+Lc/2)

1a61. By increasing the metal line length of interconnect in IC, the delay increases
A. Linearly
B. By square law
C. By 3/2 law
D. By 2/3 law
E. By cubic law

1a62. In what case is the short connection current missing in CMOS inverter?
A. $V_{tp}=V_{tn}$

B. $V_{tp}+V_{tn}=0$
C. $V_{tp}+V_{tn}<VDD$
D. $|V_{tp}|+V_{tn}<VDD$
E. $|V_{tp}|+V_{tn}<VDD/2$

1a63. Which answer is true, if $V_{IN}=V_{DD}$?



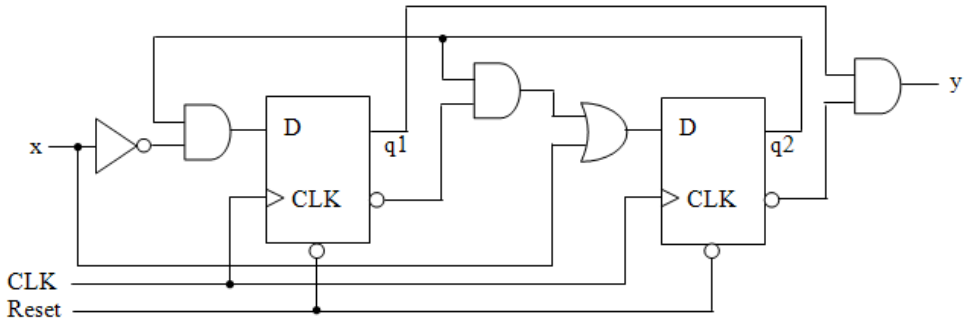
A.M1-saturated, M2-linear
B. M1-linear, M2-linear
C.M1- linear, M2- saturated
D. M1-saturated, M2-saturated
E. None

1a64. In what case is short connection current missing in CMOS inverter?
A. $V_{tp}=V_{tn}$
B. $V_{tp}+V_{tn}=0$
C. $V_{tp}+V_{tn}<VDD$
D. $|V_{tp}|+V_{tn}<VDD$
E. $|V_{tp}|+V_{tn}<VDD/2$

1a65. What equation describes JK flip-flop junctions?
A. Q+=Q&J + !Q&K
B. Q+=!Q&J + Q&K
C. Q+=!Q&J + Q&!K
D. Q+=Q&!J + !Q&K
E. Q+=Q&J + !Q&!K

1a66. At passing from one technology to the other, transistors are scaled by S <1 coefficient due to which the gate capacitance of a transistor with minimal sizes, depending on S:
A. Increases linearly
B. Decreases linearly
C. Increases by square law
D. Decreases by square law
E. Does not change

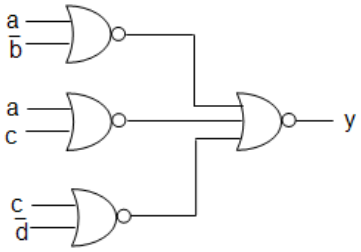
1a67. Given a circuit of synchronous FSM, detector of an input sequence. Perform FSM analysis.



Determine which input sequence the given FSM detects. The end of the previous word may be a beginning of the next one.

A. 0110
B. 1001
C. 0100
D. 1101
E. The correct answer is missing

1a68. Given a circuit in NOR basis. What function does the given circuit implement?

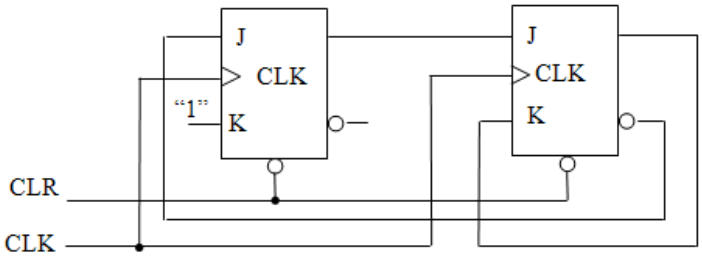


A. $\bar{a} \cdot b + \bar{a} \cdot \bar{c} + \bar{c} \cdot d$
B. $a \cdot c + \bar{b} \cdot c + a \cdot \bar{d}$
C. $b \cdot c \cdot \bar{d} + \bar{a} \cdot b + c \cdot d$
D. $\bar{a} \cdot b \cdot \bar{d} + a \cdot \bar{b} + c \cdot d$
E. The correct answer is missing

1a69. What is the difference of electrical “short” or “long” interconnects at most characterized by?

A. Interconnect width
B. Signal power
C. Signal edge increase
D. Current power
E. A. and B. together

1a70. Analyze FSM circuit, built on JK-flip-flops.



Which of the listed functions realizes the given circuit?

A. It is a modulo-4 binary up counter
B. It is a modulo-3 binary up counter
C. It is a modulo-4 binary down counter
D. It is a modulo-3 binary down counter
E. The correct answer is missing

1a71. In case of the shown element base, what is the order of power reduction of the circuit? a) bipolar; b) CMOS; c) N-MOS

A. a - c - b
B. b - c -a
C. a - b - c
D. b - a - c
E. c - b - a

1a72. Required to construct 64:1 multiplexer using 8:1 multiplexer. How many 8:1 multiplexers are needed?

A. 8 MUX 8:1

B. 9 MUX 8:1
C. 10 MUX 4:1
D. 11 MUX 8:1
E. The correct answer is missing

1a73. Which of the below listed criteria of organizing interconnects, more contributes to the increase of performance?
A. Increase of the number of interconnects layers
B. Similarity of interconnects length
C. Increase of the number of vias
D. Reduction of critical path of signal processing
E. A. and B. together

1a74. The logic of which circuit presented by VHDL code is senseless or wrong?

A.
```
process (clock)
  begin
    Y <= A and B;
  end process;
```

B.
```
process (A)
  begin
    A <= A + 1;
  end process;
```

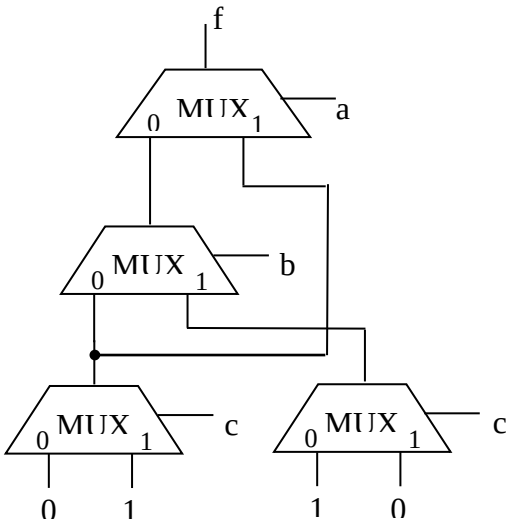
C.
```
process (A)
  begin
    Y <= A + 1;
  end process;
```

D.
```
process (A, B)
  begin
    Y <= A and B;
  end process;
```

E.
```
process (reset_n, clock)
  begin
    if (reset_n = '0') then
      Y <= 0;
    elsif (clock'EVENT and clock = '1') then
      Y <= A and B;
    end if;
  end process;
```

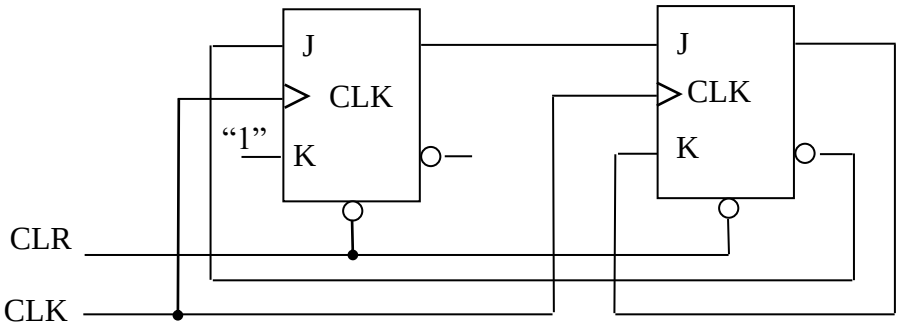
1a75. Given F(x1,x2,x3) = x1⊕ x2⊕ x2·x3 function. Which of the given expressions corresponds to the given function?
A. $F = x1 \cdot \bar{x2} + x1 \cdot x3 + \bar{x1} \cdot x2 \cdot \bar{x3}$
B. $F = x1 \cdot x2 + \bar{x1} \cdot x3 + \bar{x1} \cdot x2 \cdot \bar{x3}$
C. $F = \bar{x1} \cdot \bar{x2} + x1 \cdot x2 + x2 \cdot \bar{x3}$
D. $F = x1 \cdot \bar{x2} + x2 \cdot x3 + x1 \cdot \bar{x3} \cdot x2$
E. $F = x1 \cdot \bar{x2} + x1 \cdot x2 + x2 \cdot \bar{x3}$

1a76. Which of the functions below is realized in the given circuit on multiplexer?



A. $\bar{b}\cdot c + a\cdot c + \bar{a}\cdot b\cdot \bar{c}$
B. $\bar{a}\cdot b + b\ \bar{c} + a\ \bar{c}$
C. $a\cdot \bar{b} + a\cdot b\cdot c + \bar{b}\cdot c$
D. $a\cdot b + a\cdot b\cdot c + \bar{b}\cdot c$
E. $b\cdot c + a\cdot c + b\cdot c$

1a77. Analyze the FSM, designed on JK flip-flop.

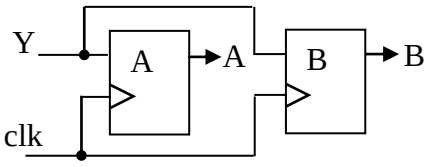


What does the given FSM represent?
A. 2-bit shift register
B. polynomial counter
C. subtractive bitwise counter modulo 4
D. additive bitwise counter modulo 3
E. subtractive bitwise counter modulo 3

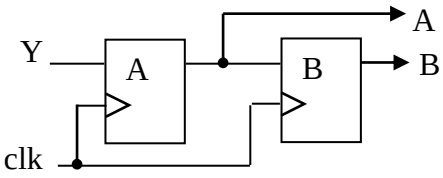
1a78. Which circuit does the use of the following assignment correspond to?

```
always  @(posedge clk)
begin
      A<=Y;
   B<=A;
end
```

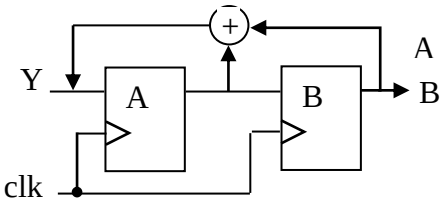
A.



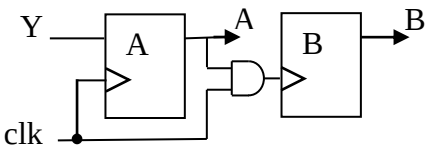
B.



C.

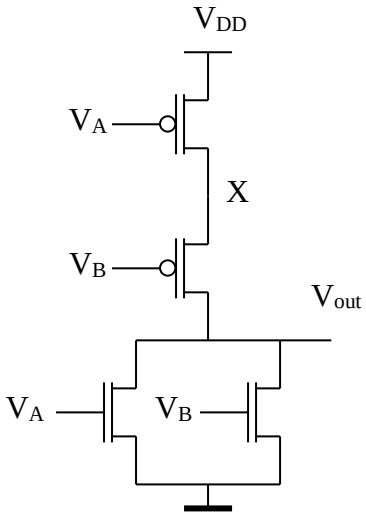


D.



E. None of the circuits corresponds to the assignment.

1a79. In case of what transition of input signal, the circuit output does not switch, and X node switches?



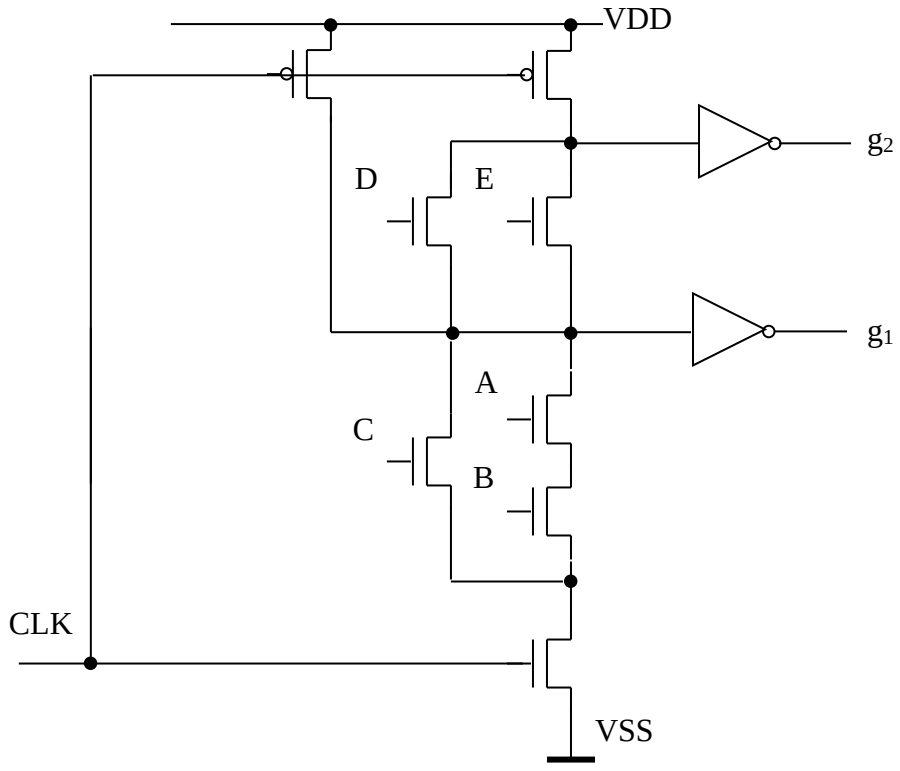
A. AB=00->01
B. AB=00->11
C. AB=01->10
D. AB=11->00
E. AB=10->00

1a80. For what purpose is created Low-Doped-Drain (LDD) region?
A. to increase threshold voltage
B.to increase saturation voltage
C. to increase gate-source break-down voltage
D. to reduce gate capacitance
E. to increase gate's oxide break-down voltage

1a81. The first stage of the 12-input 2-stage decoder is implemented by 3AND cells, and the second one - by 4AND cells. How many 3AND cells are there in the first stage?
A. 16
B. 24
C. 32
D. 8
E. 64

1a82. Considering that memory array has equal number of 1-bit cells in lines and columns, define how many word lines does 10 address bit memory has if the word length is 4 bits.
A. 32
B. 64
C. 128
D. 1024
E. 256

1a83. What logic function does the circuit implement?



A. $g_1=(A+B)C$, $g_2=(A+B)C+ED$
B. $g_1=AB+C$, $g_2=(AB+C)(E+D)$
C. $g_1=AB+C$, $g_2=(AB+C)ED$
D. $g_1=AB\oplus C$, $g_2=(AB\oplus C)ED$
E. $g_1=AB+C$, $g_2=(AB+C)\ (E\oplus D)$

b) Problems

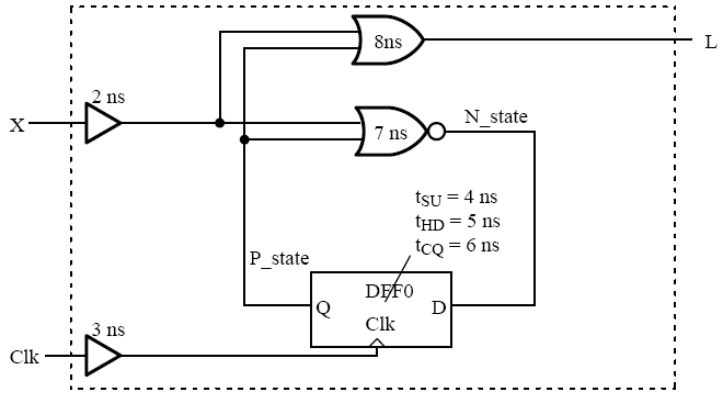
1b1.

For the shown circuit:

a. What are the external setup and hold times for input X?

b. What is the delay from the clock to output L?

c. What is the clock cycle time based on register–to–register delays? (flip flop is drawn ‘‘backwards’’).



1b2.

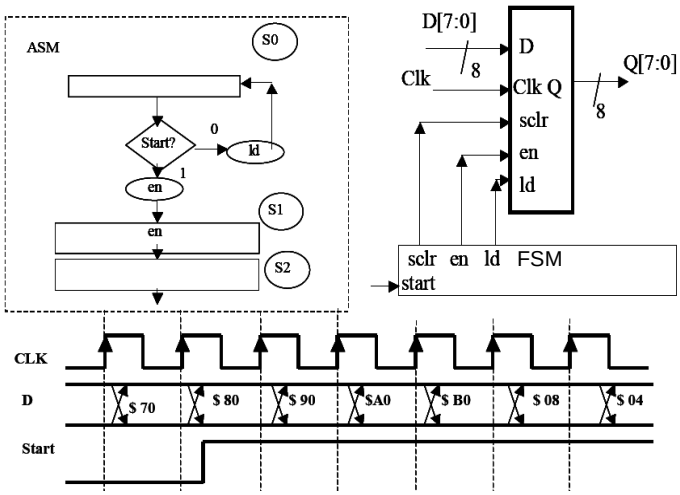
Consider the following VHDL code.

```
library ieee;
use ieee.std_logic_1164.all;
entity pulsedet is port(
signal clk,reset,pulse_in: in std_logic;
signal pulse_out: out std_logic
);
end pulsedet;
architecture behavior of pulsedet is
signal dffout : std_logic_vector(2 downto 0);
begin
dffs: process(clk,reset)
begin
if (reset = ’1’) then
dffout <= “000”;
elsif (clk’event and clk=’1’) then
dffout(2) <= dffout(1);
dffout(1) <= dffout(0);
dffout(0) <= pulse_in;
end if;
end process;
pulse_out <= dffout(2) and not dffout(1);
end behavior;
```

Draw a diagram of logic that implements the VHDL code. (Show logic gates and D flip–flops.)

1b3.

On the waveforms below, complete the waveforms for State, ld, en, and Q. The FSM is controlling the UP counter. Assume the initial state is S0.



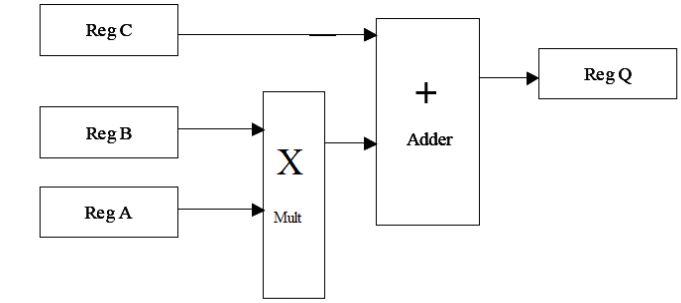
1b4.

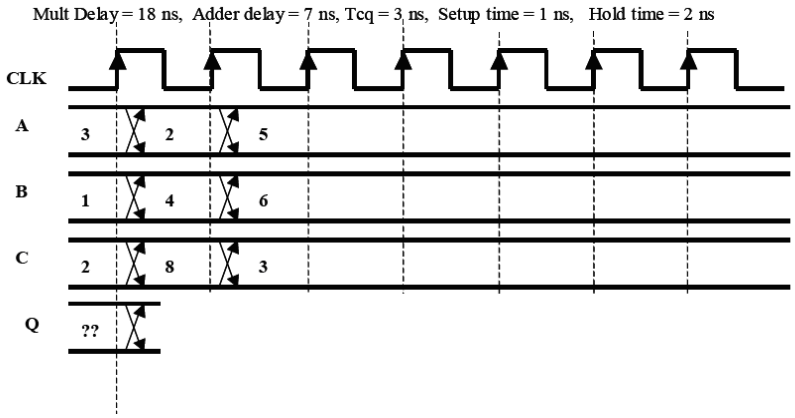
For the figure below:

a. Give the maximum register-to-register delay.

b. Modify the diagram to add one level of pipelining but still maintain the same functionality. Add the pipeline stage in the place that will improve the register-to-register delay the most. Compute the new maximum register-to-register. Assume that adding a pipeline registers to any functional unit (adder or multiplier) breaks the combinational delay path in the unit exactly in half.

c. With the pipeline stage added, complete the 'Q' waveform shown below. Input registers change values as shown; assume Reg Q is loaded every clock cycle. All waveforms represent register outputs.





1b5.

Build the circuit for CMOS cell which is realized by

$$Z=!(A(B+C)+BD)$$

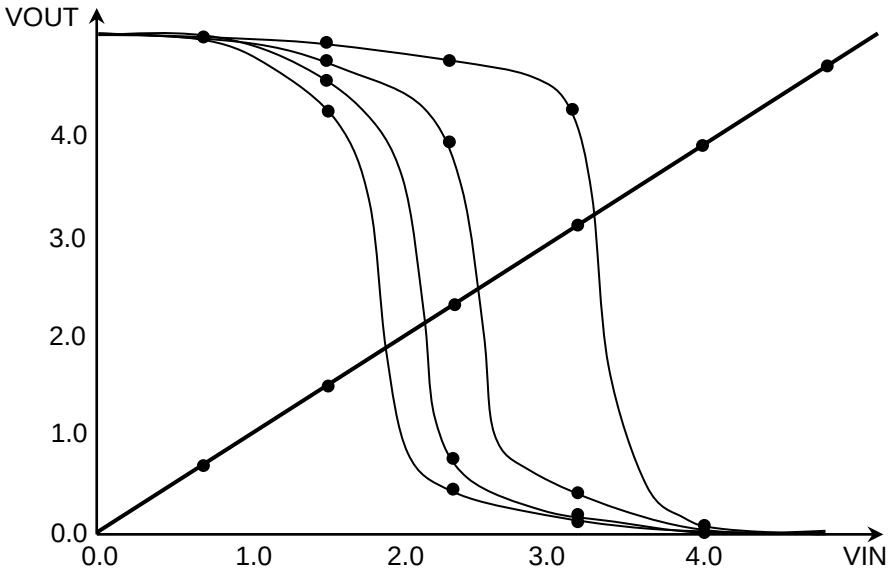
logic function.

1b6.
Build MS D-FF based on transmission gates (TG) with SET input.

1b7.
Build MS D-FF based on switching keys with SET and RESET inputs.

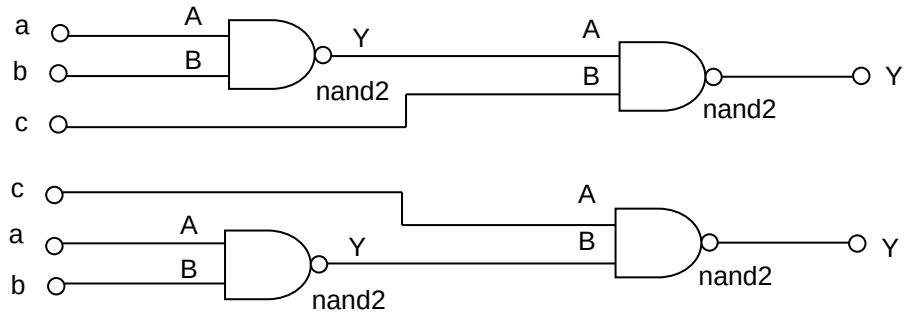
1b8.
Build CMOS cell circuit which is described by Y=∑(1,2,6,7) function.

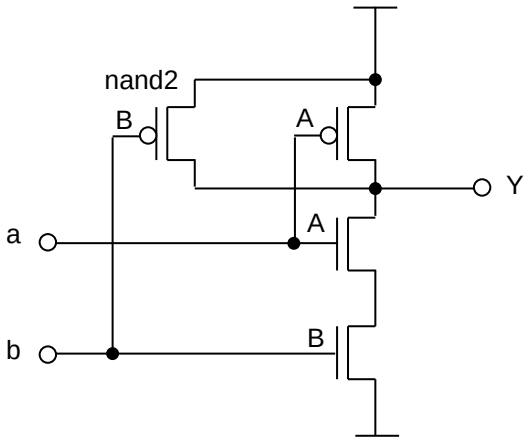
1b9.
Four inverters (VDD=5V) have WN, changing from 3um to 12um while WP is the same for each inverter (10 um).
Identify which WP/WN ratio produces the most left curve in Figure 1.
In this process VDD is 5V. Which inverter has the most even noise margins (V_{THN}=0.6 V, V_{THP}=-0.8 V, LN=LP)?



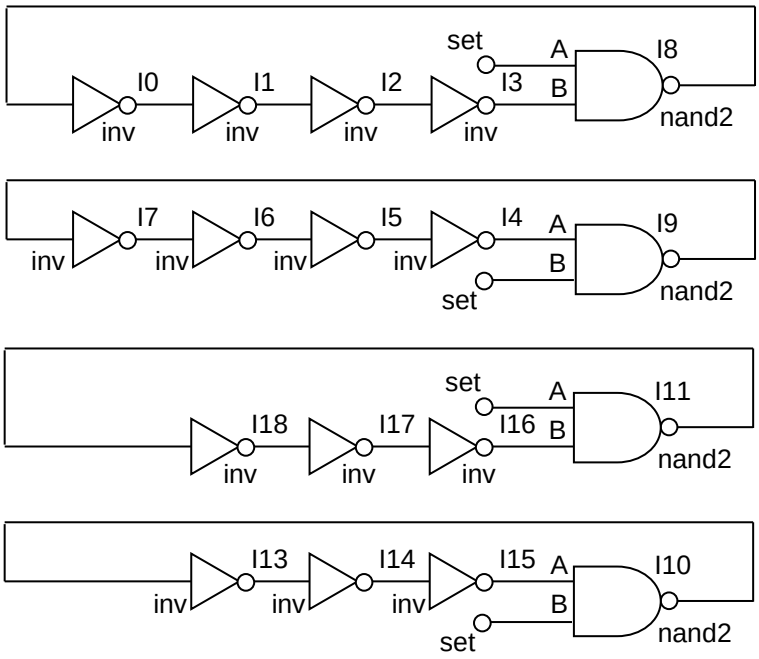
DC response of three different inverters

1b10.
Both circuits below have the same function. Which one has the smallest, best case delay? Explain the answer for full credit.

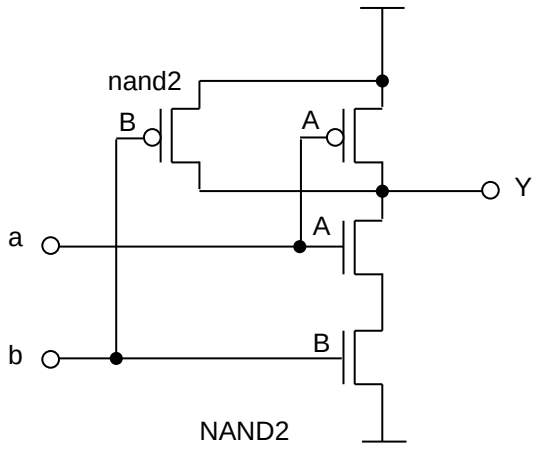




1b11.
It is necessary to design a ring oscillator that is to oscillate as fast as possible. Usually a set pin is needed to start the ring oscillator properly. Which circuit would be used for the fastest ring oscillator?
Explain why for full credit.

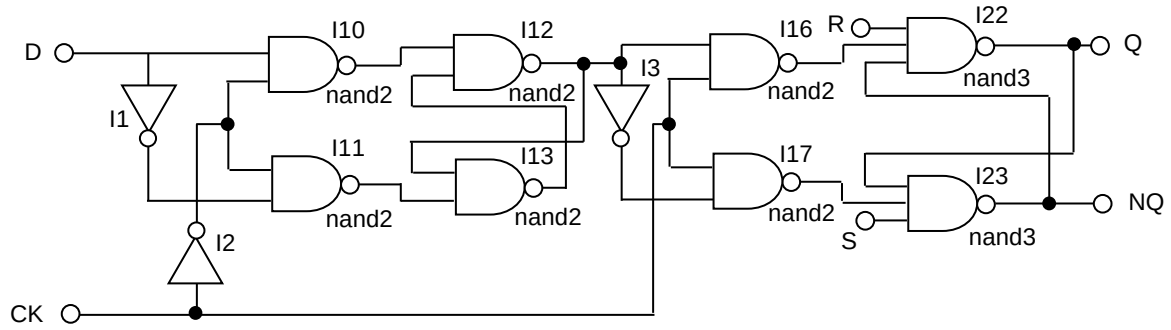


Circuits of ring oscillator



NAND2

1b12.
Figure shows a DFF. Using the timing data presented in the table, calculate how long CK has to remain high for Q and NQ to get the value from the output of I12 (nand2).
Figure shows a DFF. Using the timing data presented in the table, calculate how long D has to remain stable before the rising clock edge so that the outputs of I12 and I13 properly get the value of D (or not(D)).



DFF

Table: Various times for various gates.

	INV	NAND2	NAND3
TFALL (ps)	200	500	600
TRISE (ps)	300	500	650
τphl (ps)	100	250	300
τplh (ps)	150	250	325

1b13.
Using the AOI technique design a CMOS circuit to implement the following logic function:

Z=(ABCD+EFG)H

Show the PNET and the NNET connected into a circuit.

1b14.
Using the AOI technique, design a CMOS circuit to implement the following logic function:

Z=(AB+CD+EF)G

Show the PNET and the NNET connected into a circuit.

1b15.
Using the AOI technique, design a CMOS circuit to implement the following logic function:

Z=(AB+CD+EF)G

Show the PNET and the NNET connected into a circuit.

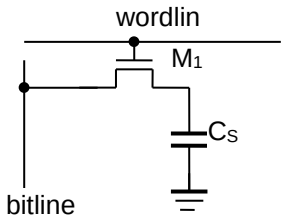
1b16.
Using the AOI technique, design a CMOS circuit to implement the following logic function: Minimize area and delay. (Show Euler path, but do not draw it).

Z=(AB+CD+EFG)H

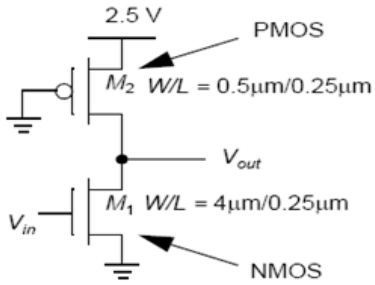
Show the PNET and the NNET connected into a circuit.

1b17.

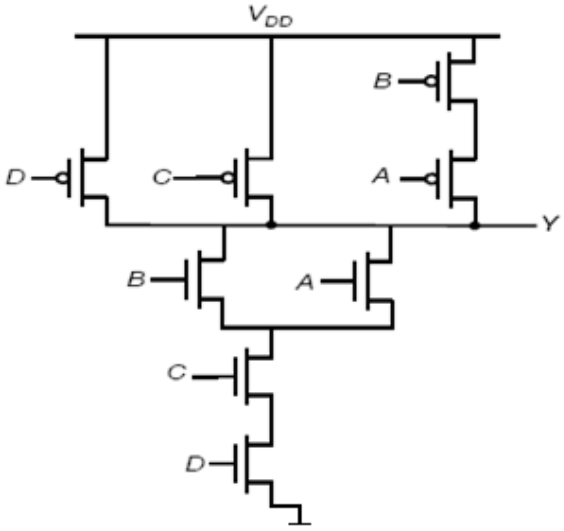
For reading the bitline is precharged to VDD/2. Determine the settled voltage on the bitline when reading logic 1 and logic 0, if Vtn=0.3V, VDD=1.2V, C_{BL}=10C_s. The voltage swing of the wordline control is from 0 to VDD. Ignore leakages and body bias effect.



1b18.
Compute the following for the pseudo-NMOS inverter shown below:
k_n = 115uA/V^2, k_p = 30uA/V^2, V_{tN} = 0.5V, V_{tP} = -0.4V
a) V_{OL} and V_{OH}
b) The static power dissipation: (1) for V_{in} low, and (2) for V_{in} high
c) For an output load of 1 pF, calculate t_{pLH}, t_{pHL} (ignore the intrinsic capacitances of transistors)

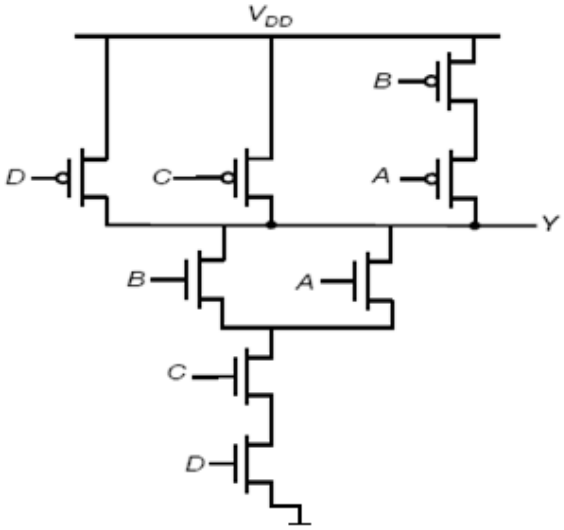


1b19.
Consider the circuit below.
a) What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS *W*/*L* = 4 and PMOS *W*/*L* = 8.
b) What are the input patterns that give the worst case *tpHL* and *tpLH*. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.



1b20.

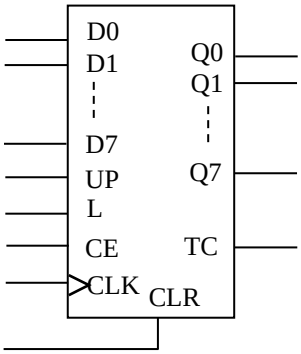
If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=0.8, determine the switching power dissipation in the logic gate. Assume *VDD*=2.5V, *Cout*=30fF and *fclk*=250MHz.



1b21.

Design 8-bit binary up/down counter with parallel synchronous loading, asynchronous reset and an input to enable counting.

Logic symbol for the given counter:



CLK – clock input
CE – count enable input
CLR – active high asynchronous reset input
L – active high synchronous load input
D0 … D7 – parallel data inputs
UP – input of count direction change
Q0 … Q7 – data outputs
TC – carry output (output of count completion)

TC is set as soon as code FF_{16} or 00_{16} appears on counter outputs.

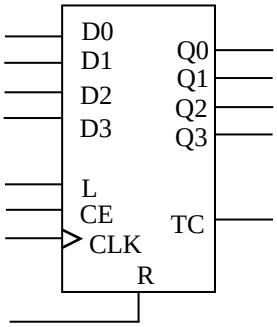
Truth table of the counter

CLR	L	CE	UP	CLK	Q7 … Q0	TC	Mode
1	X	X	X	X	0 … 0	0	Asynchronous reset
0	1	X	X		D7 … D0	0	Parallel loading (D[7:0]≠FF)
0	1	X	X		D7 … D0	1	Parallel loading (D[7:0] =FF)
0	1	X	X		D7 … D0	1	Parallel loading (D[7:0] ≠00))
0	1	X	X		D7 … D0	1	Parallel loading (D[7:0] =00)
0	0	1	1		+1	0	Increment (Q[7:0] ≠FF)
0	0	1	1		+1	1	Increment (Q[7:0] =FF)
0	0	1	0		-1	0	Decrement (Q[7:0]) ≠ 00)
0	0	1	0		-1	1	Decrement (Q[7:0]) = 00)
0	0	1	0	X	$Q7_n$ … $Q0_n$	TCn	Hold

$Q7_n$ … $Q0_n$ – previous states of the counter.

a) Describe counter in Verilog and Simulate using logic analysis tool VCS.
b) Synthesize using Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually, using T flip-flops. For simplification take the number of bits equal to 4.

1b22.
Design 4-bit binary-coded decimal counter with parallel synchronous loading, synchronous reset and count enable inputs.
Logic symbol for the given counter:



CLK – clock input
CE – count enable input
R – active high synchronous reset input
L – active high synchronous load input
D0 … D3– parallel data inputs
Q0 … Q3 – data outputs
TC – carry output (output of count completion)

TC is set as soon as code 1001_2 appears on counter outputs.

Truth table of the counter

R	L	CE	CLK	Q3 … Q0	TC	Mode
1	X	X	↑	0 … 0	0	Synchronous reset
0	1	X	↑	D3 … D0	0	Parallel loading (D[3:0]≠1001)
0	1	X	↑	D3 … D0	1	Parallel loading (D[3:0] =1001)
0	0	1	↑	+1	0	Increment (Q[3:0]#FF)
0	0	1	↑	+1	1	Increment (Q[3:0]=FF)
0	0	0	X	$Q3_n$ … $Q0_n$	TCn	Hold

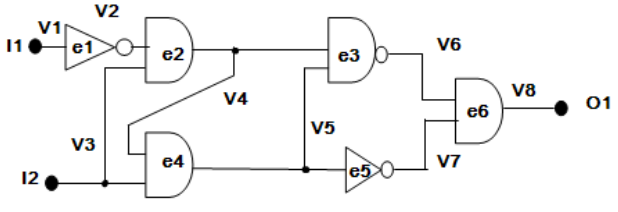
$Q3_n$…$Q0_n$ – previous states of the counter.

a) Describe counter in Verilog and Simulate using logic analysis tool VCS.
b) Synthesize using Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually, using T flip-flops.

1b23.
Design a clocked synchronous Moore FSM producing a remainder of division of a decimal number by 3 on its outputs. FSM receives the digits of a decimal number sequentially on its inputs.
a) Describe counter in Verilog and Simulate using logic analysis tool VCS.
b) Synthesize using Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually.

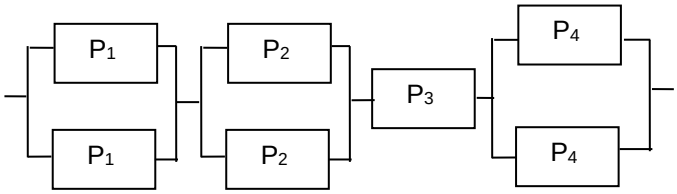
1b24.
Design a clocked synchronous FSM with two inputs, X and Y, and one output, Z. The output should be 1 if the number of 1 inputs is the multiple of 5 on X and Y since reset, and 0 otherwise.
a) Describe counter in Verilog and Simulate using logic analysis tool VCS.
b) Synthesize using Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually.

1b25.
Calculate the minimum and maximum signal formation time of the shown circuit in V_1 – V_8 nets by conventional units, if the cell delays are given by conventional units $\tau_{e1}=\tau_{e5}=10$, $\tau_{e3}=15$, $\tau_{e2}=\tau_{e4}=\tau_{e6}=20$: On the circuit mark I/O critical path and calculate the total delay of that path by conventional units.



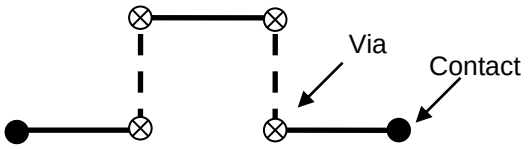
1b26.
An interconnect of 300 um length and 0,2 um width is given, the sheet resistance and capacitance of which correspondingly equal:
$R_{\square}$ =0,2 Ohm/$\square$
C =0,1 fF/um.
Construct the equivalent circuit of interconnect's 3-segment, R,C distributed parameters and calculate the delay in it.

1b27.
Calculate faultness probability of IC consisting of 7 blocks if their connection, according to reliability, has the following view.



Given P_1=0.5; P_2=0.6; P_3=0.8; P_4=0.4.

1b28.
Two contacts are connected by an interconnect containing 4 vias, as illustrated in the figure.



Construct interconnect's R, C equivalent circuit and calculate the delay in the transmission line connecting two contacts, if given:
- Each transmission line's capacitance of interconnect equals 100 fF
- Each programmable contact resistance equals 1 Ohm.

Ignore ohmic resistances of transmission lines and contacts as well as the capacitances of vias.

1b29.
Based on the logic of provided VHDL code, develop digital circuit consisting of logic gates.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity adder2 is port(
  signal
    operand1,
    operand2: in std_logic_vector(1 downto 0);
  signal
    sum: out std_logic_vector(2 downto 0);
  );
end adder2;
architecture behavior of adder2 is
begin
  sum <= operand1 + operand2;
end behavior;
```

Determine whether the provided logic is a combinational logic or not. Please argue the answer.

1b30.
Based on the logic of provided VHDL code, develop digital circuit consisting of logic gates.

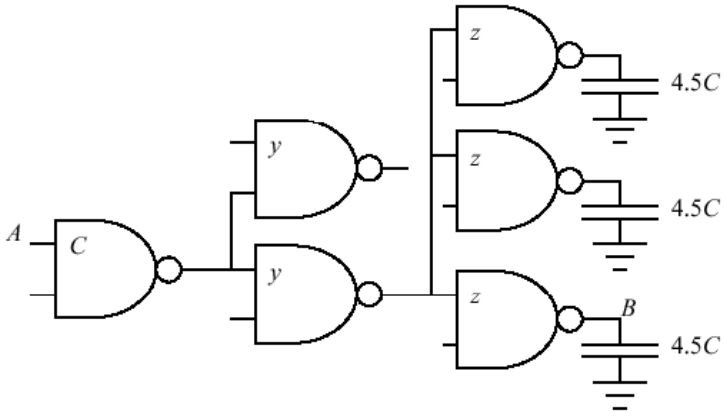
```
library ieee;
  use ieee.std_logic_1164.all;
  use ieee.std_logic_unsigned.all;
```

```
entity incr1 is port(
  signal
    operand: in std_logic_vector(2 downto 0);
  signal
    incr_result: out std_logic_vector(3 downto 0);
  );
end incr1;
architecture behavior of incr1 is
begin
  incr_result <= operand + 1;
end behavior;
```
Determine whether the provided logic is a combinational logic or not. Please argue the answer.

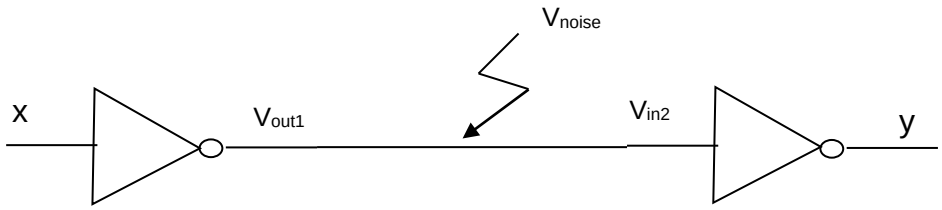
1b31.
Based on the logic of provided VHDL code, develop digital circuit consisting of logic gates.
```
library ieee;
  use ieee.std_logic_1164.all;
  library types;
  use types.conversions.all;
  entity shift_ll is port(
    signal
      operand: in std_logic_vector(3 downto 0);
      shift_size: in std_logic_vector(1 downto 0);
    signal
      shift_result: out std_logic_vector(3 downto 0);
    );
  end shift_ll;
  architecture behavior of shift_ll is
  begin
    process (operand, shift_size)
    begin
      --left logical shift by shift_size
      shift_result <= operand sll to_uint(shift_size);
    end process;
  end behavior;
```
Determine whether the provided logic is a combinational logic or not. Please argue the answer.

1b32.
Based on the logic of provided VHDL code, develop digital circuit consisting of logic gates.
```
library ieee;
  use ieee.std_logic_1164.all;
  library types;
  use types.conversions.all;
  entity shift_rl is port(
    signal
      operand: in std_logic_vector(3 downto 0);
      shift_size: in std_logic_vector(1 downto 0);
    signal
      shift_result: out std_logic_vector(3 downto 0);
    );
  end shift_rl;
  architecture behavior of shift_rl is
  begin
    process (operand, shift_size)
    begin
      --right logical shift by shift_size
      shift_result <= operand srl to_uint(shift_size);
    end process;
  end behavior;
```
Determine whether the provided logic is a combinational logic or not. Please argue the answer.

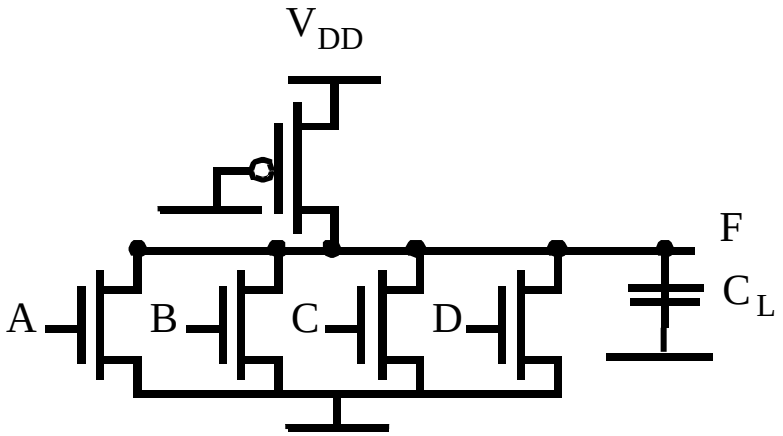
1b33.
The sizes of the first cell in the shown logic circuit are selected in a way that it has a driving strength of a minimal size inverter having input capacitance C, i.e. NMOS transistor sizes have been increased to compensate the consequence of serial connection.
Define the second and third stages' scaling ratios **y** and **z,** from the condition to get minimum delay in the A-to-B path. Ignore intrinsic output and interconnects capacitances of cells.



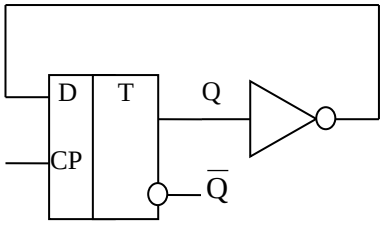
1b34.
For the following circuit define the maximum allowable noise magnitude V_{noise}, if the inverter's VTC parameters are V_{OHnom}=1V, V_{OHmin}=0.9V, V_{OLnom}=0V, V_{OLmax}=0.15V, V_{SP}=048V, V_{IHmin}=0.58V, V_{ILmax}=0.44V.



1b35.
Define four input NOR cell's output low and high levels (see the figure) (a) when only one input switches, (b) when all the inputs switch simultaneously if C_L=0.05 pF. Use the following technological parameters VDD=1.8 V, $T_{ox}=10^{-8}$ m, μ_n=270 cm²/Vv, V_{tn}=0.5V, μ_p=70 cm²/Vv, V_{tp}=-0.5V, L_n=0.18 um, W_n=20 um, Wp=5 um.

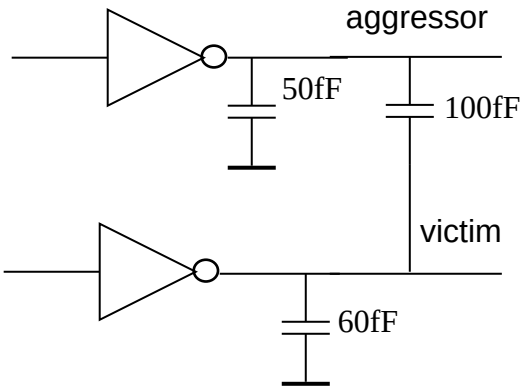


1b36.
Here a circuit of frequency divider is presented.

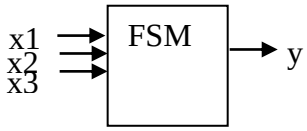


Define the minimum period of clock pulses, if t_{su}=20ps, t_{hd}=-15ps, t_{c2q}=100ps, t_{pinv}=30ps.

1b37.
For the given circuit define:
a) maximum value of the noise in the victim line, which occurs when the signal in the aggressor line switching from 1.0 V to 0V.
b) effective capacitance of victim line for delay calculation if the signals in aggressor and victim lines are switching in opposite directions.



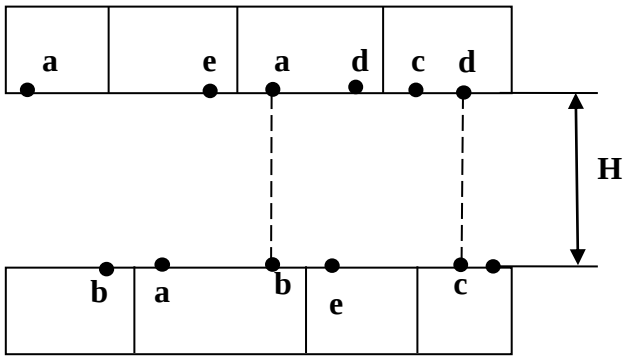
1b38.
Design Moore FSM which has 3 inputs x1, x2, x3 and 1 output. The output of FSM equals 1 when total number of ones, which are given to FSM inputs, is divided by 7.



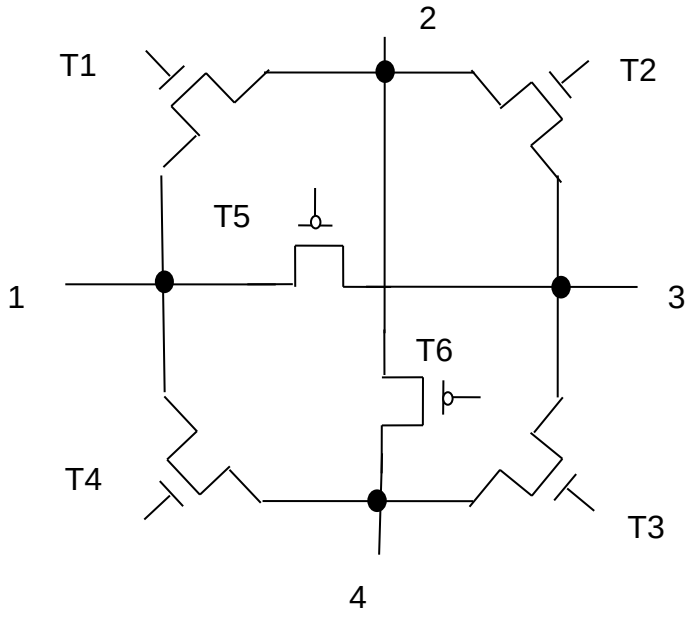
Describe on Verilog. Create a testbench and simulate using VCS.

1b39.
Describe on Verilog 5-bitpolynomial. In feedback circuit $d(x) = 1+ x^3 +x^5$ is polynomial. The counter has 10000 initial state asynchronous preset input. The shift of information is realized by positive edge of clock signal.
Describe on Verilog. Create a testbench and simulate using VCS.

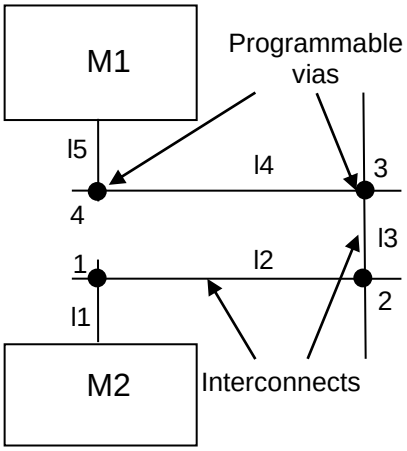
1b40.
Define the minimum H distance between two rows of cells which is necessary for routing of two-layer co-perpendicular routing of a, b, c, d, e nets if the minimum permissible size between interconnects width and space is 0,1 um, and the minimum distance between interconnects and 0,2 um.



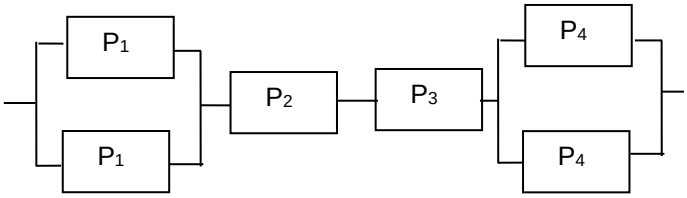
1b41.
Switching block with 4 pins (1, 2, 3, 4) is shown in the figure. It consists of 4 N-MOS and 2 P-MOS transistors. What kind of logic level signals (0 or 1)should be given to each gate of T1-T6 transistors in order to provide:
a) simultaneous signal transfer from pin 1 to 3 and from pin 2 to 4;
b) simultaneous signal transfer from pin 1 to 4 and from pin 2 to 3;



1b42.
Two modules (M1 and M2) are connected with 5 interconnects (l1-l5) and 4 programmable vias (1-4). Construct interconnect's R, C equivalent circuit and calculate the delay in the transmission line connecting two modules, if given:
Each transmission line's capacitance of interconnect equals 100 fF
Each programmable contact resistance equals 1 Ohm.
Ignore ohmic resistances of interconnects and contacts as well as the capacitances of programmable vias.



1b43.
Calculate faultness probability of IC consisting of 7 blocks if their connection, according to reliability, has the following view.



Given P_1=0,5; P_2=0,6; P_3=0,8; P_4=0,4.

2. ANALOG INTEGRATED CIRCUITS

a) Test questions

2a1. How is the balancing of the differential amplifier executed?
- *A. By applying additional biasing to one of inputs*
- *B. Through external potentiometer connected between load resistors of two branches*
- *C. By the change of supply voltage value*
- *D. A. and B. answers are correct*
- *E. All the answers are wrong*

2a2. What differences are between inverting and non-inverting adders based on operational amplifier?
- *A. Output signal's phase*
- *B. There is interaction of signal sources in inverting adder*
- *C. In inverting adder inputs are limited*
- *D. Interaction of signal sources is absent in inverting adder*
- *E. B. and C. answers are correct*

2a3. Input resistance for differential signal of differential amplifier can be increased by:
- *A. The increase of resistors in emitter circuits*
- *B. The increase of transistors'* β*s*
- *C. The application of Darlington's transistors*
- *D. The application of field transistors*
- *E. All the answers are correct*

2a4. What is the advantage of "R – 2R" matrix towards "R - 2R - 4R - 8R © © © © ©" matrix in digital-analog converters?
- *A. More precise*
- *B. Can be multibit*
- *C. The current of reference voltage is constant*
- *D. Is being heated in a more uniform way*
- *E. All the answers are correct*

2a5. Which analog-digital converter (ADC) is the fastest?
- *A. Sequential ADC*
- *B. Parallel ADC*
- *C. Double integration ADC*
- *D. The speed depends on the applied cells*
- *E. The most high-speed is not mentioned among the answers*

2a6. Why does the increase of collector resistor value lead to transistor's saturation mode in a common emitter circuit?
- *A. Because it leads to collector voltage increase*
- *B. Because it leads to base current increase*
- *C. Because it leads to collector current increase and contributes to transistor opening*
- *D. All the answers are correct*
- *E. All the answers are wrong.*

2a7. What is the differential amplifier's application limited by?
- *A. Large input resistance*
- *B. Large output resistance*
- *C. The difference of input resistances for common mode and differential signals*
- *D. Large amplifier coefficient*
- *E. All the answers are correct*

2a8. What is the reason of occurrence of disbalance of differential amplifier?
- *A. Transistors of two branches are not similar*
- *B. Difference of resistance values between two branches*
- *C. The summary difference between both transistors and resistors of two branches*
- *D. Non ideal nature of the power source*
- *E. All the answers are correct*

2a9. What properties are being demonstrated by active integrator considered from the frequency point of view?

A. High pass filter
B. Low pass filter
C. Band-pass filter
D. Rejecter filter
E. Has no filtering properties

2a10. The random variable signal conversion accuracy of ADC depends on:
A. Comparator accuracy
B. Resistors accuracy in R-2R matrix of internal DAC
C. Bit count of ADC
D. Performance of ADC elements
E. All the answers are correct

2a11. The quality of current source in differential amplifier depends on
A. High internal resistance
B. Thermostability
C. Current value
D. A, B, C answers are correct
E. A, B answers are correct

2a12. Analog IC production group method is based on the following factors:
A. Parameter similarity of elements produced during the same technological process
B. Elements on crystal, which are placed close to each other, heat evenly
C. Elements thermal coefficient similarity
D. A, B, C answers are correct
E. Technological restrictions on element implementation

2a13. What is the minimum value of the resistance of OpAmp negative feedback limited by?
A. Ku=1 request
B. Thermal instability of input current
C. Permissible minimum value of resistance of OpAmp output load
D. No limitation
E. All the answers are wrong

2a14. In voltage stabilizer by OpAmp application why is the feedback given to the inverse input not from OpAmp output, but from the output of output emitter repeater
A. To fade the loading of OpmAmp
B. To fade stabilitron current given to the direct input
C. To compensate thermal instability of the output emitter repeater
D. To increase amplifier's coefficient of OpAmp
E. All the answers are correct

2a15. What factors is the redundancy principle of analog microcircuitry based on?
A. Technological restrictions of element preparation
B. On those elements of the circuit which are not possible to carry out in crystal or occupy too much area, are substituted by multielement node which implements the same function.
C. A.and B. answers are correct
D. On placing redundant elements on crystal area
E. Minimization of the number of circuit elements

2a16. Why does not the emitter oscillate the voltage?
A. Because the output voltage must always be smaller than the one of the input for open state of the transistor
B. Because it is not possible to increase large nominal resistance in emitter circuit
C. Because the output signal is taken from transistor's emitter
D. Because the emitter repeater cannot provide large output resistance
E. All the answers are correct

2a17. What is the role of additional emitter repeater in current mirror?
A. Has no influence
B. Increases the output current of current mirror
C. Balances current mirror
D. Increases the output resistance of current mirror

E. All the answers are wrong

2a18. What is the comparator's sensibility, built on OpAmp, conditioned by?
A. Input resistances of OpAmp
B. Value of supply voltage
C. Own amplifier's coefficient of OpAmp
D. Debalance of OpAmp
E. All the answers are wrong

2a19. What is the advantage of double integration of ADC?
A. Increases the conversion accuracy
B. Thermal stability
C. Compensates the thermal instability of integrator's capacitor
D. A., B. answers are correct
E. A., B., C.answers are correct

2a20. Between what points is the input resistance for differential signal of differential amplifier distributed?
A. Between inputs of differential amplifier
B. Between inputs of differential amplifier and ground
C. Between one input of differential amplifier and ground
D. Between one input of differential amplifier and negative power source
E. All the answers are wrong

2a21. In what state are bipolar transistor's junctions in saturation mode?
A. Emitter junction is close, collector - open
B. Emitter junction is open, collector - close
C. Both junctions are open
D. Both junctions are close
E. Saturation mode has no connection with the states of junctions

2a22. Why is not resistance applied as stable current source in differential amplifier?
A. Large resistances, characteristic of current source, are not possible to realize in semiconductor ICs
B. Large voltage drop is obtained on the resistance of large nominal, which leads to the increase of power supply voltage value
C. The resistance cannot be current source at all
D. A., B. answers are wrong
E. All the answers are wrong

2a23. What is the function of the output cascade of OpAmp?
A. Current amplifier
B. Power amplifier
C. Provides small output resistance
D. B., C. answers are correct
E. All the answers are wrong

2a24. Why with bipolar transistors, minimum values of output signals of differential amplifier for small signal application are limited by approximately -0.7V level?
A. Due to one of transistors falling into saturation mode
B. Due to one of transistors collector opening
C. Due to closing of one of transistors
D. A., B. answers are correct
E. Due to value limitation of collector resistance

2a25. What should the structure of MOS transistor look like to reduce body effect?
A. Square of the bulk diffusion must be large
B. Bulk diffusion must be rounded over transistor.
C. Bulk diffusion must be as close to the transistor as possible
D. A and C answers are correct
E. B and C answers are correct

2a26. What signals are the switching capacitances controlled by?
A. Overlap clock signals

B. Clock signals
C. Multi-level clock signals
D. Non overlap clock signals
E. Non clock signals

2a27. Which ADC is principally the fastest?
A. Sigma-delta
B. Dual slope integrating AC
C. SAR
D. Integrating
E. Pipeline

2a28. How can the channel modulation effect of a MOS transistor be reduced?
A. By decreasing bulk potential
B. By decreasing transistor's L
C. By decreasing transistor's W
D. By increasing transistor's W
E. By increasing transistor's L

2a29. How much is the NMOS source follower output voltage, when the input transistor is in saturation mode?
A. Equal to supply voltage
B. Equal zero
C. Larger than input voltage by threshold voltage of input transistor
D. Smaller than input voltage by threshold voltage of input transistor
E. Equal to input voltage

2a30. What is the advantage of using field transistor in the input of DiffAmp?
A. Input capacitance decreases
B. Input resistance increases
C. Input offset error decreases
D. Has no advantage
E. A, B and C answers are correct

2a31. Which of the listed ADC contains DAC?
A. SAR
B. Flash
C. Integrating
D. Dual slope integrating
E. All the answers are correct

2a32. By what element is channel modulation of MOS transistor presented in a small signal model?
A. Controlled voltage source
B. Resistance
C. Controlled current source
D. Capacitor
E. RC circuit

2a33. The effect of what errors reduces in Pipeline ADC's digital correction application
A. Errors, which depends on Gain of OpAmp
B. Errors which depends on Capacitor values scaling
C. Comparators offset error
D. Comparators sensitivity
E. C and D answers are correct

2a34. Which of the mentioned DAC is not used in ICs?
A. R-string DAC
B. R-2R DAC
C. Charge scaling DAC
D. Current DAC
E. All are used

2a35. What is the ICs life time conditioned by?
A. Supply voltage value
B. Migration

C. Leakage power
D. Maximum clock frequency of IC
E. All the answers are correct

2a36. By what element is the body effect of a MOS transistor presented in a small signal model?
A. Controlled voltage source
B. Resistance
C. Controlled current source
D. Capacitor
E. RC circuit

2a37.What is the minimum value of OpAmp's negative feedback limited by?
A. Input resistance of OpAmp
B. Amplifying coefficient of OpAmp
C. Minimum value of OpAmp's output load resistance
D. A=1 value
E. Minimum value of OpAmp's input current

2a38. What is the reason of differential amplifier's debalance?
A. Non similarity of diffpair (transistor)
B. Accuracy of current source
C. Loads non matching
D. A and B answers are correct
E. A and C answers are correct

2a39. How many comparators does 8 bit two-stage Flash ADC contain?
A. 15
B. 30
C. 255
D. 31
E. 63

2a40. How many comparators does the single-stage 8-bit Flash analog to digital converter have?
A. 31
B. 7
C. 255
D. 63
E. 127

2a41. What is the main disadvantage of a SAR analog to digital converter?
A. limited accuracy
B. low performance
C. A and B answers are correct
D. A, B and E answers are correct
E. thermal instability

2a42. What the high performance of ADC is conditioned by?
A. high performance of input switches
B. output change rate of output operational amplifier
C. converter's capacity
D. A, B and C answers are correct
E. A and B answers are correct

2a43. Why are differential amplifiers applied only in case of high ohmic loads?
A. because they have two outputs
B. because the reduction of load resistance reduces the amplification coefficient of differential signal
C. because the reduction of load resistance leads to amplification of common-mode signal
D. B, C and D answers are correct
E. B and C answers are correct

2a44. Why aren't differential amplifiers used as a standalone amplifiers?
A. because of too high output resistance
B. because can't work with low ohmic loads

C. because amplifiying of differential signal changes wuth laod resistance
D. A, B and C answers are correct
E. A and B answers are correct

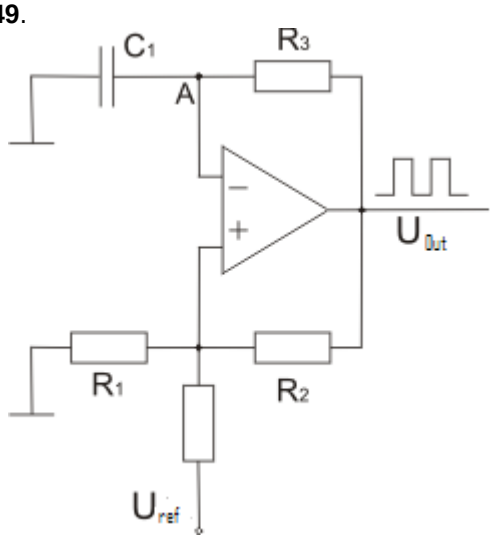
2a45. What is body affect in a small signal model of a MOS transistor presented by?
A. current controlled current source
B. voltage controlled voltage source
C. voltage controlled current source
D. resistance
E. current controlled voltage source

2a46. By what is channel length modulation in a small signal model of a MOS transistor presented?
A. current controlled current source
B. voltage source
C. capacitor
D. resistor
E. current controlled voltage source

2a47. What is the body effect of a MOS transistor conditioned by?
A. potentials' difference of source and drain
B. potentials' difference of source and gate
C. potentials' difference of drain and substrate
D. potentials' difference of gate and substrate
E. potentials' difference of source and substrate

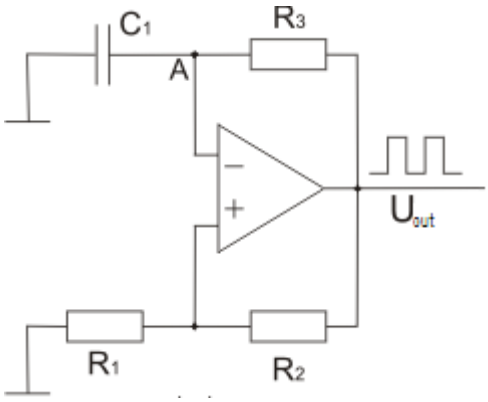
2a48. What is the channel length modulation of a MOS transistor conditioned by?
A. potentials' difference of source and drain
B. potentials' difference of source and gate
C. potentials' difference of drain and substrate
D. potentials' difference of gate and substrate
E. potentials' difference of source and substrate

2a49.



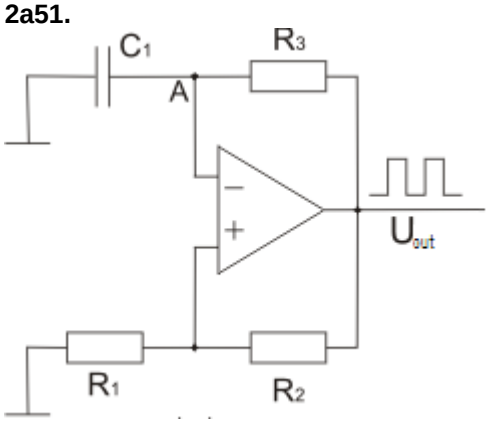
How will the change of R1 affect this generator?
A. output amplitude will change
B. output frequency will change
C. amplitude at point A will change
D. frequency at point A will change
E. all the answers are wrong

2a50.



How will R1 change affect this generator?
A. the amplitude of output pulses will change
B. the frequency of output pulses will change
C. the amplitude of A point pulses will change
D. the frequency of A point pulses will change
E. B, C and D answers are correct

2a51.



The change of which element of this generator will lead to the change of frequency of output signal?
A. R_2
B. R_3
C. C_1
D. B and C answers are correct
E. A, B and C answers are correct

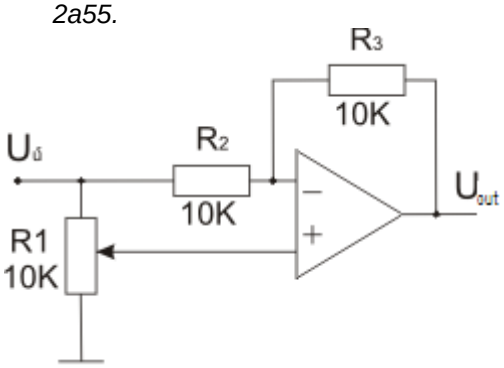
2a52. Between which pins of a MOS transistor there is no direct capacitance?
A. source and gate
B. drain and gate
C. gate and substrate
D. source and substrate
E. source and drain

2a53. How can the conductance of a MOS transistor change in case of the given technology and gate source voltage? (ignore secondary effects)
A. changing gate drain voltage of a transistor
B. changing drain source voltage of a transistor
C. changing the sizes of channel
D. not possible to change
E. changing the sizes of source and drain

2a54. What does the MOS transistor in saturation mode represent?

A. current source
B. voltage source
C. linear resistance
D. resistance
E. infinite small resistance

2a55.



Within what limitations will U_{output} voltage change when moving control of R_1 potentiometer form min position to max position

A. from U_m to $2U_m$
B. from $-U_m$- to $-2U_m$
C. from $-2U_m$ to U_m
D. from $-U_m$- to U_m
E. from $-U_m$- to $2U_m$

2a56. What is the accuracy of digital-analog converter with R-2R matrix conditioned by?

A. accuracy of making matrix resistors
B. the value of voltage offset error of output OpAmp
C. the gain of output OpAmp
D. A and B answers are correct
E. A, B and C answers are correct

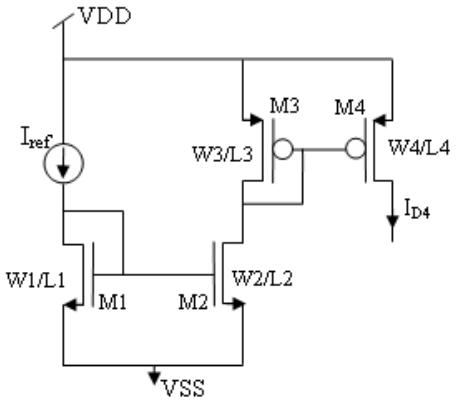
2a57. How can amplifying coefficient of single stage common source resistive load amplifier be increased?

A. increasing resistance value
B. increasing channel width
C. increasing channel length
D. A and B answers are correct
E. A and C answers are correct

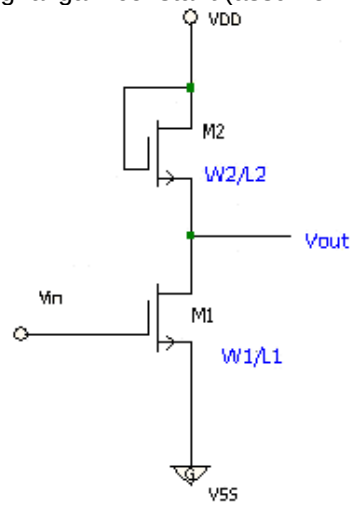
b) Problems

2b1.

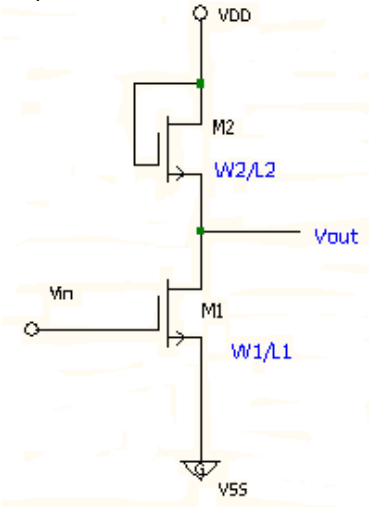
For the following circuit find $I_{D4}=f(I_{ref})$ dependence if $\lambda=0$, $L_1=L_2=L_3=L_4$, $W_1=W_2$, $W_3=W_4$. Consider all the transistors are in saturation mode.



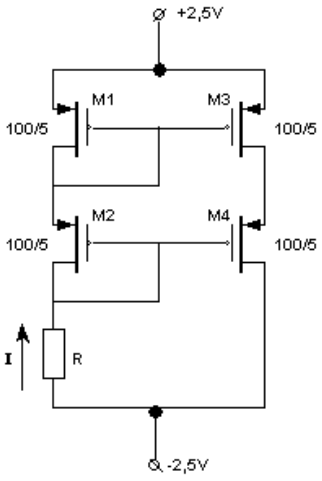
2b2.
For the following circuit define small signal gain constant (assume M1 is saturated and λ=0, γ=0).



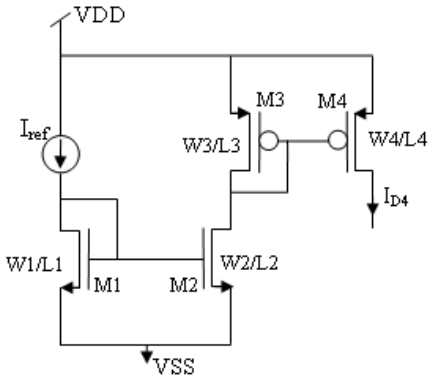
2b3.
For the following circuit define the value of input voltage in case of which M1 is out of saturation mode, if $(W/L)_1$=49 $(W/L)_2$=9 V_{TH}=0.7 VDD=3, λ=γ=0.



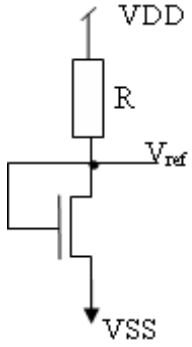
2b4.
A current mirror is given by transistors' geometrical sizes. Find the gate voltage of M1 transistor.



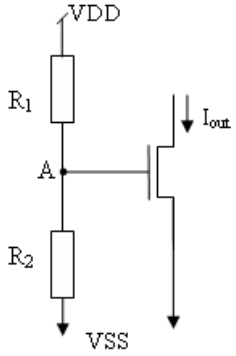
2b5.
For the following circuit find the drain current of M4 transistor if all the transistors are in saturation. Ignore channel length modulation (λ=0).



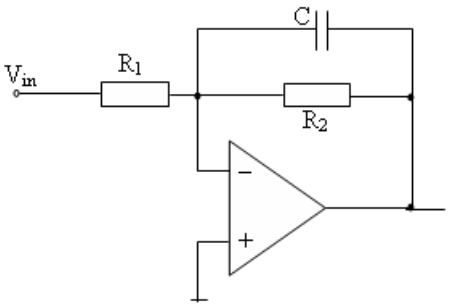
2b6.
For the following circuit find V_{ref}, if μ_n=550 cm^2/Vs, ε_{Si02}=3.9, ε_0=8.85*10^{-14} F/cm, t_{ox}=0.16 nm, V_{thn}=0.8V, V_{DD}=2V, V_{SS}=0V, W=L=10 um, λ=0, R=10 kOhm.



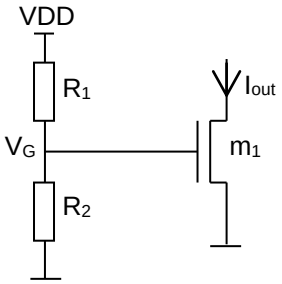
2b7.
For the following circuit define how much I_{out} will change if V_{DD} changes by ± 10% and if the transistor is in saturation and W=50um, L=0.5um, I_{out}=0.5mA, K_n=120 uA/V^2, V_{TH}=0.5V VDD=3V, (nominal value), R_2/R_1=0.35, λ=0.



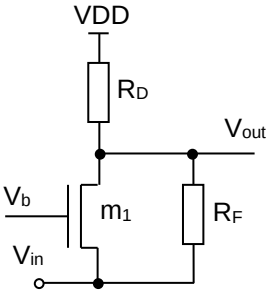
2b8.
Find the cutoff frequency of the following circuit and build amplitude-frequency characteristics, if R_1, R_2 and C are known.



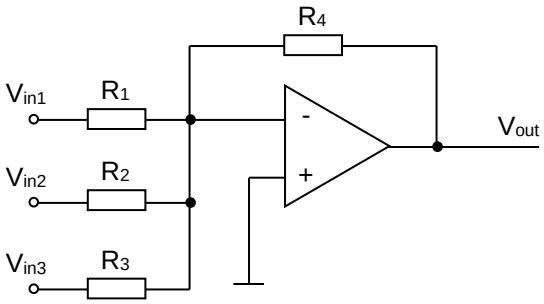
2b9.
What does I_{out} equal when the transistor is in saturation (express transistor's conductivity by g_m). Ignore body effect and channel modulation.



2b10.
Find V_{out} depending on V_{in}, if the transistor is in saturation. Ignore body effect and channel modulation.

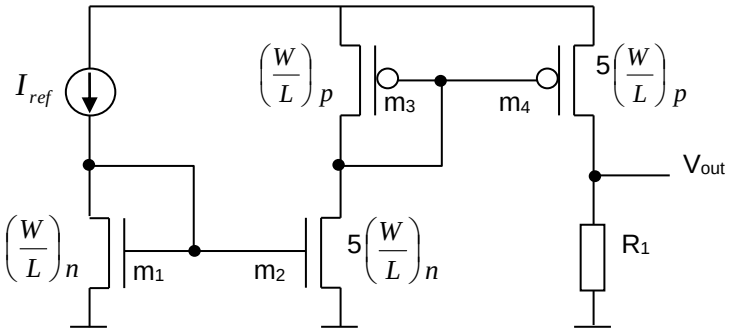


2b11.
R1, R2, R3, R4 resistances are given. Find $V_{out} = f(V_{in1}, V_{in2}, V_{in3})$, considering the real K_A amplifying coefficient.



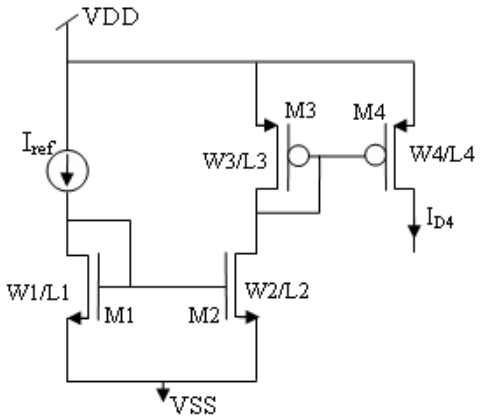
2b12.

$\left(\frac{W}{L}\right)n$, $\left(\frac{W}{L}\right)p$, I_{ref}, R_1 values are given. Find V_{out}, ignore channel modulation.



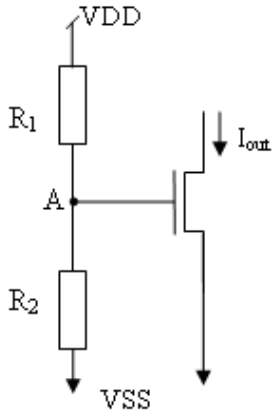
2b13.

For the folowing circuit find the $I_{D4}=f(I_{ref})$ dependence, if $\lambda=0$, $L_1=L_2=L_3=L_4$, $W_1=W_2=3W_3=6W_4$. All transistors are saturated.



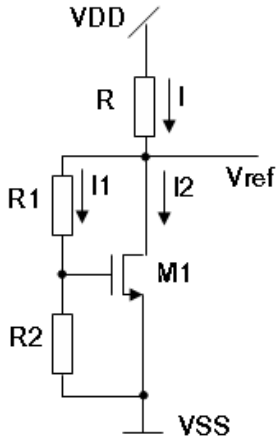
2b14.

Calculate how much will Iout change, if VDD increase by 10%: Given W, L, μ_n, V_{TH}, C_{OX}, R_2, R_1. Transistor is saturated, secondary effects can be neglected.



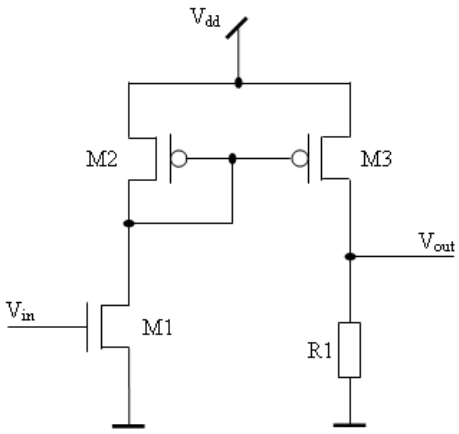
2b15.

Calculate the value of R, if M1 transistor is saturated and given are VDD, Vref, V_{TH}, β, R_1, R_2, λ=0:



2b16.

Find $k = \frac{dV_{out}}{dV_{in}}$ coefficent (by variable component). Given $g_{m1}, g_{m2}, g_{m3}, R$.



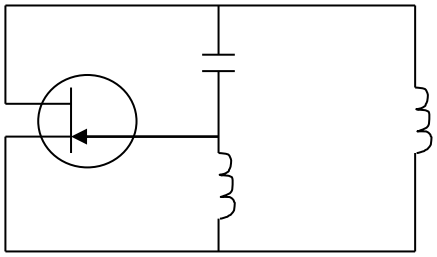
3. RF CIRCUITS

a) Test questions

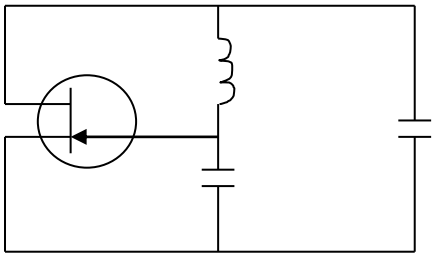
3a1. Define super-heterodyne receiver's intermediate frequency if the input signal frequency is fs = 900 MHz, and heterodyne frequency is fh = 700 MHz

A. 200 MHz
B. 600 MHz
C. 1400 MHz
D. 1600 MHz
E. 1800 MHz

3a2. Which of the shown circuits is called "Inductive triple point"?



A.



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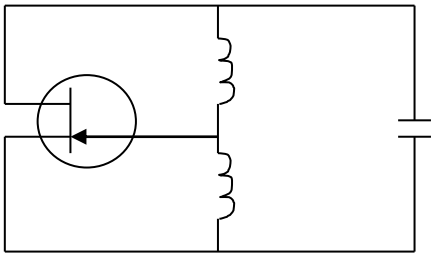
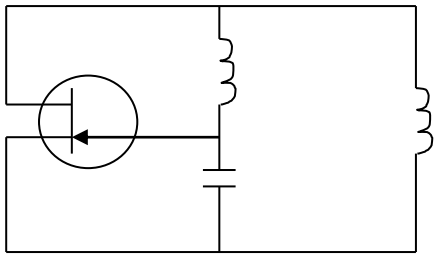
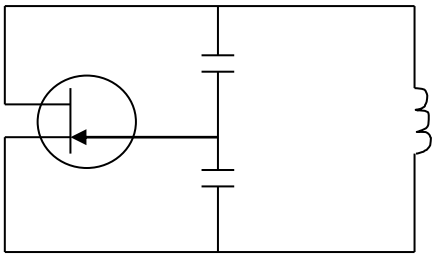


C.



D.



E.

3a3. Find the initial phase of second harmonic of the following signal:

$$s(t)=\sum_{n=1}^{2}\frac{2}{n}\cos\left[2\pi n\cdot 10^{6}t+\frac{\pi}{n}(-1)^{n+1}\right]$$

A. $-\pi$

B. $-\frac{\pi}{2}$

C. 0

D. $\frac{\pi}{2}$

E. π

4. SEMICONDUCTOR PHYSICS AND ELECTRONIC DEVICES

a) Test questions

4a1. Which circuit based on operational amplifier has transfer function with hysteresis?
- *A. Non-inverting amplifier*
- *B. Inverting adder*
- *C. Comparator without feedback*
- *D. Comparator with positive feedback*
- *E. Comparator with negative feedback*

4a2. Does semiconductor diode's I/V characteristics differ from I/V characteristics of ohmic resistance?
- *A. Yes, it depends on the applied voltage direction and is nonlinear*
- *B. Yes, it depends on the applied voltage direction and is linear*
- *C. No, as the more direct voltage, the more is the current*
- *D. Partially, as current exists irrespective of voltage direction*
- *E. The correct answer is missing*

4a3. What parameters of semiconductor material are needed for transistor fabrication?
- *A. Charge carriers' mobility and concentration*
- *B. Charge carriers' concentration, minority charge carriers' life time, mobility*
- *C. Charge carriers' concentration and diffusion coefficient*
- *D. Charge carriers' concentration, diffusion coefficient, mobility, band gap*
- *E. The correct answer is missing*

4a4. Which regions does the graph of drain current dependence on source-drain voltage for p-n junction field effect transistor consist of?
- *A. Linear dependence, saturation*
- *B. Linear dependence, saturation, breakdown*
- *C. Linear dependence, transition, saturation, breakdown*
- *D. Linear dependence, transition, breakdown*
- *E. The correct answer is missing.*

4a5. In what way are the oxide layer capacitor C_0, the surface state capacitor C_{ss} and the differential capacitor of the surface charge layer connected between each other in MOS structure?
- *A. Css and C_0 parallel, and with Csc sequentially*
- *B. Css and Csc parallel, and with C_0 sequentially*
- *C. C_0 and Csc sequentially, and with Csc parallel*
- *D. All capacitors are connected parallel to one another*
- *E. The correct answer is missing.*

4a6. How does differential resistance of p-n junction change parallel to direct current increase?
- *A. Does not change*
- *B. Decreases*
- *C. Increases*
- *D. Increases, then decreases*
- *E. The correct answer is missing*

4a7. How many times will diffusion capacitance of bipolar transistor increase if its base length is increased twice?
- *A. Will not change*
- *B. Will increase $\sqrt{2}$ times*
- *C. Will increase 4 times*
- *D. Will decrease twice*
- *E. The correct answer is missing*

4a8. How does the p-n-p bipolar transistor's transfer factor depend on diffusion length of holes L_p
- *A. No dependence*
- *B. Increase with increase of L_p by $\beta = 1 - \frac{W}{2L_p}$ law*

C. *Increase with increase of* L_p *by* $\beta = 1 - \frac{1}{2}\left(\frac{W}{L_p}\right)^2$ *law*

D. *Decreases*

E. *The correct answer is missing*

4a9. The light of what maximum wavelength can influence the current of silicon ($E_g = 1.1$ eV) photodiode?

A. $\lambda_{max} = 1130$ *nm*

B. $\lambda_{max} = 550$ *nm*

C. $\lambda_{max} = 1240$ *nm*

D. $\lambda_{max} = 335$ *nm*

E. *The correct answer is missing*

4a10. How is bipolar transistor's current gain expressed in common base circuit with the help of emitter effectiveness γ, transition coefficient β and collector's avalanche multiplication factor *M* ?

A. $\alpha = \frac{\gamma\beta}{M}$

B. $\alpha = \gamma\beta M$

C. $\alpha = \frac{M}{\gamma}\beta$

D. $\alpha = \frac{\beta}{\gamma M}$

E. *The correct answer is missing*

4a11. Is operating temperature range of ICs, computers and other semiconductor devices conditioned by the used semiconductor material's band gap?

A. *Yes, the more the band gap, the more temperature range*

B. *No, as concentration of minority charge carriers is independent from temperature*

C. *Conditioned partially as by increasing the temperature carriers' mobility decreases*

D. *No, as band gap does not depend on temperature*

E. *The correct answer is missing above*

4a12. Which expression is wrong?

A. *Diode subtypes are: point-junction diodes, stabilitrons, varicaps and tunnel diodes.*

B. *In tunnel diodes reverse current for the same voltage is higher than direct current value.*

C. *In varicaps with increase of voltage barrier capacitance increases.*

D. *Schottky diodes operation is based on processes which take place in semiconductor-metal contact.*

E. *The response time of Schottky diodes, therefore, frequency properties are conditioned by barrier capacitance.*

4a13. Field effect transistors, compared with bipolar transistors

A. *Have small input resistance*

B. *Have small noise coefficient*

C. *The current is at the same time conditioned by electrons and holes*

D. *Provides current amplification*

E. *The performance is mainly conditioned by injection of minority carriers*

4a14. Through which device is the electrical signal amplification implemented?

A. *Resistor*

B. *Capacitor and inductor*

C. *Diode*

D. *Transistor*

E. *Photodiode*

4a15. How many pins does the field effect transistor have?

A. *1 gate*

B. 2 sources and 1 drain
C. 3 sources, 1 gates and 1 drain
D. 2 bases and 1 collector
E. 1 source, 1 gate and 1 drain

4a16. Is the gate of field effect transistor isolated from its channel?
A. Yes
B. No
C. Partially and there is weak tunnel coupling
D. In saturation mode of field effect transistor most part of channel current flows through gate
E. The correct answer is missing

4a17. n – type Ge sample, which is anticipated for making a transistor, has 1.5 Ohm·cm specific resistance and $5.4 \cdot 10^3$ cm^3/Kl Holy coefficient. What is the charge carriers' concentration and their mobility equal to?
A. $1.6 \cdot 10^{21}$ m-3, 5 $m^2/V \cdot s$
B. $1.6 \cdot 10^{21}$ m-3, 0.1 $m^2/V \cdot s$
C. $1.16 \cdot 10^{21}$ m-3, 0.36 $m^2/V \cdot s$
D. $2 \cdot 10^{20}$ m-3, 0.36 $m^2/V \cdot s$
E. The correct answer is missing.

4a18. By means of what semiconductor device can light influence be detected?
A. Posistor
B. Resistor
C. Photodiode
D. Capacitor
E. Inductor

4a19. Which materials' conductivity is higher?
A. Dielectrics'
B. Semiconductors'
C. Metals'
D. All have low conductivity
E. *All have low* conductivity

4a20. How does the negative differential resistance current range change depending on the density of lightly degenerated n-region impurities in tunnel diode?
A. The interval decreases when increasing the density
B. The interval increases when increasing the density
C. It is not conditioned by the density of the impurity
D. The interval increases when reducing density
E. All the conditions are true

4a21. Generally, what is the response time of photodiode conditioned by?
A. The diffusion time of equilibrium carriers in the base
B. Their transit time through the layer of p-n junction
C. RC constant of diode structure
D. Only A and C
E. Conditions A, B, C

4a22. Which statement mentioned below is not true for ohmic contact?
A. Electrical resistance of ohmic contact is small
B. Electrical resistance of ohmic contact does not depend on the current direction if the current value does not exceed the given value
C. Electrical resistance of ohmic contact does not depend on the current direction in case of any current value flowing through it
D. Most part of ohmic contacts is formed on the basis of n-n+ or p-p+ type contacts
E. All the answers are correct

4a23. By increasing the lifetime of electrons 4 times, their diffusion length
A. Increases 4 times
B. Increases twice
C. Does not increase

D. Reduces twice
E. The correct answer is missing

4a24. What does the generation frequency depend on in Gunn diode?
A. Mobility speed of field domain
B. Impurity density in semiconductor
C. Sample length
D. Dielectric permeability of material
E. All the answers are correct

4a25. How can the cutoff voltage of MOS transistor change?
A. By opposite voltage of substrate-channel junction, when substrate is more high ohmic than the channel
B. By opposite voltage of substrate-channel junction, when substrate resistance is equal or smaller than the channel resistance
C. By voltage applied to the gate
D. By A and C
E. By B and C

4a26. Which statement is wrong for unipolar transistors?
A. In unipolar transistors, physical processes of current transport are conditioned by one sign carriers-electrons or holes
B. In unipolar transistors, physical processes of current transport are conditioned by the injection of minority carriers.
C. In unipolar transistors current control is carried out by the vertical electrical field
D. The surface channel unipolar transistor includes metal-dielectric-semiconductor structure
E. The correct answer is missing

4a27. What is the high frequency property of Schottky diode conditioned by?
A. Moving the majority carriers through the diode
B. Excluding minority carriers' accumulation in the diode
C. Value of Schottky *barrier*
D. Impurity density in a semiconductor
E. Only C and D

4a28. Which of the below written statements is wrong for an integrated capacitor?
A. Integrated capacitor represents IC element consisting of conductive electrodes (plates), divided by isolation layer
B. In ICs the role of integrated capacitor is often performed by reverse-biased p-n junctions of transistor structure
C. The quality factor of integrated capacitor is defined by the following:

$$Q = 2\pi f RC$$

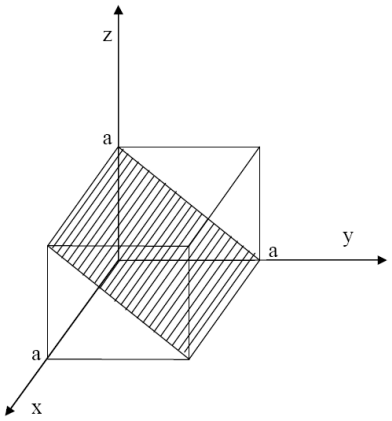
where f *– operating frequency,* C *– capacitance of a capacitor,* R *– resistance of a resistor sequentially connected with the transistor*
D. The quality factor of integrated capacitor characterizes loss of power at capacitive current junction
E. All the answers are correct

4a29. Which of the below mentioned statements is wrong for electronic lithography?
A. In this method as a source of radiation the electron beams are used
B. The method of electron beam lithography is based on non-thermal influence left by electron beam on resist
C. At electron beam lithography the ultraviolet beams fall on resist surface
D. In electron beam lithography method it is possible to reduce diffraction effects by increasing the electron accelerating voltage
E. The correct answer is missing

4a30. Which of the below mentioned statements is right for bipolar transistor being in saturation mode?
A. Emitter and collector junctions are forward-biased
B. Emitter junction is forward-biased, and collector junction –reverse-biased
C. Transistor base resistance in this mode is maximum, as emitter and collector junctions inject large number of free particles to base region

D. Free carriers' extraction takes place from transistor base being in this mode
E. The correct answer is missing

4a31. What crystallographic plane is underlined in cubic lattice?



A. (100)
B. (101)
C. (001)
D. (011)
E. (110)

4a32. Due to what below mentioned properties is currently silicon considered the main material of microelectronics?
A. Exclusive combination of its band gap and electro-physical parameters
B. Its oxide stability and isolating properties
C. High development of technological methods related to it in different physics-chemical processes
D. The value of its natural resources
E. All the answers are correct

4a33. What statement is wrong for metal-nitride-oxide semiconductor (NMOS) field effect transistor?
A. In such transistor, silicon nitride and silicon dioxide double structure serves as a subgate isolator.
B. There are many deep levels (traps) for electrons in silicon nitride layer
C. The layer's thickness of silicon dioxide is selected so that it is not tunnel transparent
D. After removing the voltage on MNOS-field transistor's gate, the injected charge remains long trapped, which corresponds to the existence of induced inversion layer.
E. The correct answer is missing

4a34. If the density of semiconductor's defects is large,
A. The lifetime of carriers will be large
B. Conductivity of semiconductor will decrease
C. Recombination speed will increase
D. The current will remain constant
E. Generation speed will increase

4a35. The performance of tunnel diodes is larger than the one of p – n junction as
A. Injection level is large
B. Injection mechanism is different
C. Junction capacitance is small
D. Current is formed by electrons and holes
E. Potential barrier's height is small

4a36. What diode is called stabilitron?
A. Direct current of which exponentially increases with the voltage
B. Reverse current of which is saturated
C. Reverse branch of its the volt-ampere characteristic has a region very strict dependence of current on voltage
D. The volt-ampere characteristic of which has an N- type region
E. The correct answer is missing

4a37. Threshold voltage of short channel MOS transistor is smaller than the one of MOS by long channel as
A. It occupies smaller area
B. The number of technological processes is small
C. Gate controls smaller number of charge
D. On the boundary of oxide-semiconductor junction there are piled charges
E. Intrinsic capacitance is large

4a38. In Gann diode, negative conductivity occurs
A. Due to ohmic property of contacts
B. When p-n junction is controlled by larger voltage
C. Due to field domain
D. Carriers' flight time is small
E. No answer is correct

4a39. In order to increase the MOS transistor's drain conductance which statement below is wrong?
A. It is necessary to reduce channel length and increase its width
B. It is necessary to increase the thickness of subgate isolator
C. It is necessary to use dielectric with more dielectric permittivity
D. It is necessary to use as a transistor's substrate a semiconductor with more carrier's mobility
E. The correct answer is missing

4a40. How does base volume resistance affect on semiconductor's diode characteristic?
A. It leads to the sharp increase of the current
B. The direct current, depending on the voltage, increases slower than exponential law
C. Volt - ampere characteristic, starting with the smallest value of voltage, becomes ohmic
D. Negative differential conductance region appears on volt-ampere characteristic of the diode
E. The correct answer is missing

4a41. Carriers' mobility, depending on temperature, changes:
A. Increases linearly
B. Decreases exponentially
C. Remains constant
D. Changes nonlinearly
E. No answer is correct

4a42. The reduction of oxide layer's thickness in MOS transistor leads to:
A. Increase of transistor's performance
B. Decrease of transistor's performance
C. Increase of intrinsic capacitance
D. Increase of leakage currents
E. Decrease of occupied area

4a43. Numbers of basic equivalent minimums of silicon and germanium conduction bands correspondingly are
A. 6 and 6
B. 6 and 4
C. 6 and 8
D. 4 and 6
E. 2 and 4

4a44. The band gap of semiconductor with the increase of magnetic field
A. Increases linearly
B. Increases exponentially
C. Decreases linearly
D. Decreases exponentially
E. Remains unchanged

4a45. Fermi level of full compensated semiconductor at 0K temperature is located on:
A. Middle of conduction band bottom and donor level
B. Middle of donor and acceptor levels
C. Middle of band gap
D. Donor level
E. Acceptor level

4a46. Two contacting semiconductors are in equilibrium if
A. forbidden band gaps are equal
B. Fermi levels are equal
C. free carriers concentrations are equal
D. current carriers lifetimes are equal
E. current carriers diffusion coefficients are equal

4a47. If Fermi and donor levels are equals then probability of electron occupancy in donor level is
A. 1/2
B. 1
C. 2/3
D. 1/3
E. 0

4a48. Fundamental parameters of the semiconductor are
A. electron effective mass
B. electron and hole lifetimes
C. electron and hole mobility
D. resistivity
E. coefficient of lattice thermal conductivity

4a49. P-n junction potential barrier under influence of absorbing light
A. increases
B. increases, then decreases
C. decreases, then increases
D. decreases
E. remains unchanged

4a50. When p–n junction occurs, which part of it acquires i–type conductivity?
A. High ohmic part outside p-n junction
B. contact domain of p– and n– parts
C. deep domains of p– and n– parts
D. the layer of spatial charges the layer of p-n junction
E. possible high ohmic part, adjacent to ohmic contact.

4a51. When p–n junction occurs, which flow of carriers gives rise to potential barrier?
A. diffusion of majority carriers of p– and n– domains
B. drift of minority carriers of p– and n– domains
C. two flows together
D. only diffusion of electrons
E. only drift of holes

4a52. In case of being connected by general base of bipolar transistor, when injection is missing from emitter, mainly on what part does the voltage, supplying collector p–n junction, fall?
A. on the part of load resistance, connected to collector.
B. on the layer of drift charges of collector p–n junction.
C. on both A and B.
D. on high ohmic part of collector contact.
E. on the part outside spatial charges of a collector.

4a53. What is comparably high temperature stability of a field transistor conditioned by?
A. reverse bias voltage of gate
B. possibility of modulation of channel resistance
C. output current conditioned by majority carriers
D. Both B and C
E. quality of ohmic contacts

4a54. How does the drain current of a filed transistor change when increasing the temperature?
A. increases on the account of getting rid of surface state electrons
B. decreases due to decreasing carriers' mobility
C. both A and B occur
D. does not change
E. increases together with output contact heating

4a55. What is the high performance of Schottky diode conditioned by?
A. output operation of semiconductor
B. lack of minority carriers' accumulation in a semiconductor
C. moving of majority carriers conditioned by diode operation
D. presence of charge capacitance
E. output operation of metal

4a56. Why is the lightdiode's radiation spectrum not strictly onewave?
A. Because radiation reunion of carriers occurs between two levels
B. Because radiation reunion of carriers occurs between electrons which are on one group of levels and holes which are in another group
C. Because spectral distribution of radiation, coming from diode changes
D. Because it is conditioned by injection of carriers
E. Because reunion is missing in p-n junction.

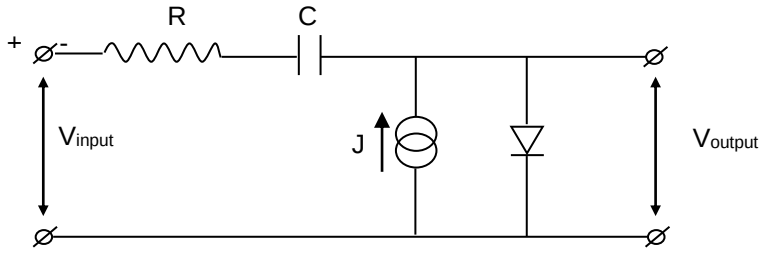
4a57. When does a semiconductor amplifier, having positive feedback, become a generator?
A. when the mirrors, creating positive feedback, provide pure reflection.
B. when amplification exceeds all the losses of radiation in the device.
C. when radiation losses in unit length of active layer are minimum.
D. when radiation is directed.
E. when radiation is provided in the layer of p–n junction.

b) Problems

4b1.

Semiconductor diode is often used in reducers as a variable resistor (see the circuit). In that case the diode's bias is given by means of J constant current source, and the connection between input and output signals is realized by the help of C capacitance, the reactive resistance of which is relatively smaller compared with R resistance.

Calculate and draw the dependence on J current expressed in decibels according to voltage signal depletion ($20\lg(V_{output}/V_{input})$), when the current ranges from 0.01 mA to 10 mA. Use $R=10^3$ Ohm in calculations, and diode saturation current $J_s=10^{-6}$ A.



4b2.

Calculate the capacitance of p-n junction, which is characterized by linear distribution of impurities: $N_A - N_D = kx$, where $k = 10^{10}$ m^{-1}, $\varepsilon\varepsilon_0 = 200$ pF/m, junction area $A=10^{-7}$ m^2, the difference of contact potential Ψ= 0.3V, and the opposite deflection V= 5V.

4b3.

Field transistor's n –channel of p^+-n - junction is characterized by arbitrary distribution of channel width impurities $N_D(x)$. Show that the transconductance of such transistor $\rho_m = \dfrac{\partial I_D}{\partial V_G}$ equals

$$\rho_m = \frac{2z\mu}{L}\left[Q(h_2) - Q(h_1)\right],$$

where h_1 and h_2 is depletion layer width at source and drain, accordingly, and

$$Q(y) = e\int_0^y N_D(y)dy\,,$$

z is channel width, L – its length, and $\mu = const$ - electron mobility.

4b4.
The semiconductor, the Holy constant of which equals 3.33*10^{-4} m/Cl, and specific resistance 8.93*10^{-3} Ohm.m, is located in magnetic field, the induction of which equals 0.5 Tl. Define the Holy angle.

4b5.
On the photovoltaic cell, the integral sensibility of which is 100 uA/lm, 0.15 lm light flow falls. Resistor with 400 kOhm resistance is successively connected to the photovoltaic cell, the signal on which is given to the amplifier, which in its turn is controlled by 10 mA current and 220 V voltage controlling relay. Define gain constant according to voltage and power.

4b6.
The ideal diode the opposite saturation current of which is 8 uA, is successively connected to 10 V emf and 1 kOhm resistor. At room temperature define diode's direct current and voltage drop on it.

4b7.
In a field transistor, the maximum value of channel current equals 2 mA, gate cutoff voltage - 5 V. Define channel current and slope of transistor characteristic in case of the following voltage values of the gate: a) -5 V, b) 0 V, c) -2,5 V.

4b8.
Silicon p-n junction is given. Define p-n junction layer's
a. d_p and d_n widths of both common *d* and *p* & *n regions*,
b. contact φ_c difference of potentials,
if the following is known:
Intrinsic charge density of silicon $n_i = 1{,}4 \cdot 10^{10}$ cm^{-3},
Dielectric transparency of vacuum $\varepsilon_0 = 8{,}85 \cdot 10^{-14}$ F/cm,
Dielectric transparency of silicon $\varepsilon = 12$,
Electron charge $q = 1{,}6 \cdot 10^{-19}$ coulomb,
Boltzmann constant $k = 1{,}38 \cdot 10^{-23}$ J/ ^{0}K,
Temperature $T = 300K$,
Conductances in n and p regions $\sigma_n = 10$ Ohm.cm and $\sigma_p = 5$ Ohm·cm,
Mobility of electrons and holes $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, $\mu_p = 500 \frac{cm^2}{V \cdot v}$:
Impurity atoms in the given temperature are considered fully ionized.

4b9.
Define silicon ideal p-n junction photodiode's
a. j_S density of saturation current,
b. open circuit $V_{o.c}$ voltage,
If the following are given:
$n_i = 1{,}4 \cdot 10^{10}$ cm^{-3}, $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, $\mu_p = 500 \frac{cm^2}{V \cdot v}$, $kT = 0{,}026$ eV, $q = 1{,}6 \cdot 10^{-19}$ q,
$N_1 = 10^{15}$ cm^{-3}, $N_3 = 5 * 10^{15}$ cm^{-3}, $L_n = 100$ um, $L_p = 60$ um, absorption coefficient $\alpha = 10^3$ cm^{-1}, base width $W = 100$ um, external quantum output $\beta = 0.7$, light sensitive area $S = 10^{-4}$ cm^2, intensity of absorbed rays^a $\Phi = 10^{18} \frac{q}{cm^2 \cdot V}$.
Accept the impurity atoms as ionized.

4b10.
Field effect silicon transistor with n-type channel and contrary p-n junctions is given.
Define

a. h_1/h_2 ratio of h_1 and h_2 widths of the channel near the source and drain,

b. *cutoff voltage*,

if given. $\varepsilon = 12$, $\varepsilon_0 = 8{,}85 \cdot 10^{-14}$ F/cm, the voltage applied to p-n junction from the supply source of the drain, near the source $V_1 = 0{,}5$ V, near the drain $V_2 = 1$V, the voltage applied to the gate V_g=0.5V, $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, $\rho_h = 5$ Ohm.cm, channel length $\ell = 10^{-2}$ cm, channel thickness $\alpha = 2{,}5 \cdot 10^{-4}$ cm, channel width $b = 10^{-2}$ cm.

4b11.
Field effect transistor with isolated gate is given which has built-in silicon n channel.
Define

a. C capacitance of the gate in depletion mode,

b. cutoff voltage V_{g0},

if given. Thickness of isolator $d = 0{,}5 \cdot 10^{-4}$ cm, $\varepsilon = 12$, $\varepsilon_0 = 8{,}85 \cdot 10^{-14}$ F/cm, $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, channel length $\ell = 10^{-2}$ cm, width $b = 10^{-2}$ cm, thickness $\alpha = 2 \cdot 10^{-4}$ cm, electron charge $q = 1{,}6 \cdot 10^{-19}$ cl, voltage applied to the gate $|V_g| = 3$ V, voltage applied to the drain – 1V, density of energetic states in conducting band $N_C \approx 10^{19}$ cm^{-3}, position of Fermi level $E_C - E_F = 0{,}2$ V, thermal energy $kT = 0{,}025$ eV.

4b12.
The barrier capacitance of an abrupt p-n junction is 200pF, when 2V reverse bias is applied towards it. What kind of reverse bias is required to apply in order to reduce its capacitance up to 50pF if the contact potential difference is $\varphi_k = 0.82$ V.

4b13.
The conductivity of n-type channel of a field effect transistor, controlled by p-n junction, is 32 Ohm^{-1} m^{-1}.The channel width is w = 8 μ m, when "gate-source" voltage equals zero. Find the "pinch-off" voltage of transistor's channel if the mobility of electrons is 2000cm^2 /V.v, and the dielectric constant of the semiconductor equals 13.

4b14.
It is known that the electrical field in the short channel field effect transistor can reach up to several kV/cm, in case of which the carriers are "heated", and their mobility becomes dependent on the electric field strength ε . Considering that the dependence has the following form:

$$\mu = \frac{\mu_n}{1 + \frac{\varepsilon}{\varepsilon_c}}$$

(μ_n - low field mobility of electrons, ε_c -critical value of electrical field) find the drain current dependence on its and the gate's voltages. Also consider that the channel length, width and depth are given.

4b15.
Boron diffusion is provided from a "limited source" with the total amount of impurities $Q = 2{,}25 \cdot 10^{13}$ atom/cm² in $t = 2$ hour. Diffusion coefficient equals $D = 9{,}2 \cdot 10^{-13}$ cm²/s. Diffusion is provided into the bulk silicon substrate with the impurity concentration $N_D = 1 \cdot 10^{16}$ atom/cm³. Calculate the depth of p-n junction x_j in micrometers.

4b16.
Consider a $p^+ - n - p$ silicon transistor with doping levels of emitter, base and collector $N_{AE} = 5 \cdot 10^{18}$ cm^{-3}, $N_{DB} = 10^{16}$ cm^{-3}, $N_{AK} = 10^{15}$ cm^{-3}, base width $W = 1$ μm, cross sectional area is 3 mm^2, and applied voltages are $U_{EB} = +0.5$ V, $U_{BK} = -5$ V. Calculate the width of quasi-neutral part of the base, minority carriers' (holes) concentration near the emitter-base junction and total charge of minority carriers injected into the base (T=300K).

4b17.
Calculate the bipolar diffusion coefficient of current carriers in intrinsic GaAs at 300K if electron and hole mobilities are equal 8800cm²/V.s and 400cm²/V.s, correspondingly.

4b18.
Find the potential barrier's height existing for electrons in Schottky diode, if the specific resistance of semiconductor $\rho = 1$ $Om \cdot cm$, electrons' mobility 3900 $cm^2/V \cdot s$, gold work function $\phi_{Au} = 5$ eV, semiconductor's electron affinity ` $\chi_{Ge} = 4$ eV, intrinsic concentration $n_i = 2.5 \cdot 10^{13}$ cm^{-3}, band-gap width $E_g = 0.66$ eV (T=300K).

4b19.
For an ideal p-n-p transistor, the current components are given by $I_{¿p}$=3mA, $I_{¿n}$=0.01mA, $I_{ïp}$=2.99mA, I_{cn}=0.001mA. Determine:
a) the emitter efficiency (γ),
b) the base transport coefficient (È$_T$),
c) the common-base current gain È$_0$ and I_{cB0}.

4b20.
In n-channel n⁺-multicrystal S_i-S_iO_2-S_i MOS transistor $N_a = 10^{17}$cm^{-3}, $(Q_{ox}/Q) = 5*10^{11}$cm^{-2}, calculate the threshold voltage V_T, if the oxide layer thickness is 5nm. What density of Bor ions is necessary to increase the threshold voltage up to 0.6V?
$2\psi_B$=0.84V, ε_{Si02}=3.9, ψ_S=-0.98V, ε_{Si}=11.9.

4b21.
Intrinsic Ge is in 3000 K temperature. How many percent will the specific conductance of the sample change if the temperature increases by 1%. Accept $\Delta E = 0.72¿ì$.

4b22.
Given mobilities of electrons and holes $(\mu_n$ ¨ $\mu_p)$, find the concentration of charge carriers corresponding to minimal specific conductance.

4b23.
How will charge carrier's lifetime in non-generated semiconductor change under the doped impurity concentration if it is known that T =3000K is constant, the mobility increases by 5%, and diffusion length decreases by 10 %.

4b24.
Using hydrogen atom model, calculate in semiconductor InSb crystal
a) donors' ionization energy,
b) the radius of electrons in basic state,
c) the electron concentration density T = 4° K, when Nd = 1 . 1014 cm^{-3}.

The radius of basic orbits is $r_H = 0.53\overset{o}{A},$ and bandgap of InSb Eg = 0.18eV, $\varepsilon_s = 17,\ m^* = 0.014m_o,$ (m_o is free electron mass), $kT = 0.0258$ eV when T = 300 K, and ionization energy E_H = 13.6 eV.

4b25.
What number of electrons must pass from one metal to another for Vk=1V contact potential difference occurs between them when the width of dielectric between metals is d=10^{-9} m, $\varepsilon_o = 8.85 \cdot 10^{-14}$ F/cm. Compare the amount when there is metal-n type semiconductor contact for the same condition when in the surface of metal, concentration of electrons is $n_{sm} \approx 10^{25}$ c^{-2}, and in semiconductor $n_{ss} \approx 10^{10}$ cm^{-2}.

4b26.
(n - p - n) transistor circuit connected by general emitter is shown. Calculate, according to power, amplification coefficient, if
$\alpha = 0.98,\ r_e = 20$ Ohm, $r_b = 500$ Ohm, $R_L = 30$ kOhm

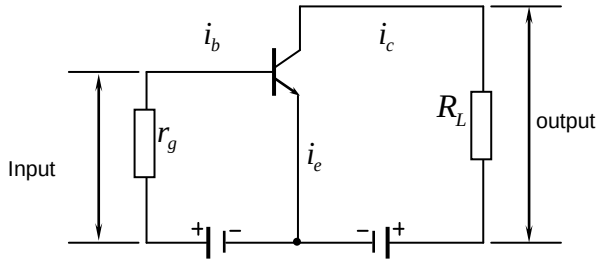


Fig.

4b27.
In the intrinsic semiconductor electron concentration is 1.3×10^{16} cm^{-3} at 400K and 6.2×10^{15} cm^{-3} at 350K. Determine the forbidden band gap of material if it changes linearly via temperature.

4b28.
Determine the holes distribution in the n-type thin and long non-degenerated germanium wire in the case of point stationary injection of holes at point $x = 0$. Electric field intensity applied on the sample is $E = 5$ V/cm, temperature is $T = 300$ K, hole diffusion length is $L_p = 0.09$ cm.

4b29.
From the plane $x = 0$ of homogeneous half-infinite ($x \geq 0$) n-type semiconductor injected holes are stationary. Determine hole current density at x=0 point if $\Delta p(0) = 10^{13}$ cm^{-3}, hole diffusion length is $L_p = 0.07$ cm, hole diffusion coefficient is $D_p = 49$ cm^2/s, injection coefficient is $\xi = 0.4$. Non-equilibrium carrier drift is neglected.

4b30.
The N type silicon sample has 4mm length, 1,5mm width, 1mm hight and 80 Ohm resistivity. Determine the acceptor concentration of the sample if 0.12m^2/Vc and 0.025m^2/Vc are the electron and hole mobilities, respectively, 2.5×10^{16}m^{-3} is the intrinsic concentration of current carrier.

4b31.
In the photodetector by surface p-n junction, the width of active layer, creating photocurrent, is d=1um, F=10^{14}quantum/cm^2·s, by $\alpha = 10^4$cm^{-1} and $\alpha = 10^3$cm^{-1} absorption coefficients, double wave (λ_1 and λ_2) radiation ($h\nu \geq E_g$) are absorbed by photosensitive surface. Calculate the photocurrent ratio, created by those two wave absorption if photosensitive area is S = 10^{-4} cm^2, quantum output β =1, electron charge q=$1.6 \cdot 10^{-19}$c.

4b32.

Define the performance of photodiode if volume charge layer width is $d=10^{-4}$ cm, maximum speed of carriers' movement $V_{max} = 5 \cdot 10^6$ cm/s, electron density in n-type base $n = 5 \cdot 10^{15} cm^{-3}$, mobility $\mu_n = 1{,}3 \cdot 10^3$ $cm^2/V \cdot s$, diffusion coefficient of minority carriers - holes D_p= 15,6 cm^2/v, Holes mobility in base $\mu_p = 600$ cm^2/Vv, electron charge $q = 1.6 \cdot 10^{-19}$c, base width $w = 3 \cdot 10^{-3}$cm, photosensitive area $S = 10^{-2}$ cm^2, dielectric permeability of semiconductor $\varepsilon = 12$, vacuum $\varepsilon_0 = 8.86 \cdot 10^{-14}$ f/cm.

4b33.
Define power density equivalent to photodiode noise if dark and light current sum $I=I_d+I_L=5{,}1 \cdot 10^{-7}$A, frequency band Δf =1Hz, absorption radiation power $P = 10^{-6}$ Vt, photocurrent $I_È=5 \cdot 10^{-7}$A, photosensitive surface $S = 10^{-2}$ cm^2, electron charge $q = 1.6 \cdot 10^{-19}$c.

4b34.
Define channel width shrinkage through p-n junction at the drain of field transistor, when source-drain domain affects are missing, V=+0.5 V voltage has been applied to the drain, dielectric permeability of channel material ε=12, vacuum ε_0=$8.86 \cdot 10^{-14}$ f/cm, contact difference of potentials φ=0.7V, donors' density in and n-channel $N_d=5 \cdot 10^{14} cm^{-3}$, electron charge $q = 1.6 \cdot 10^{-19}$c.

5. SEMICONDUCTOR TECHNOLOGY

a) Test questions

5a1. What is the number of photomasks defined by during the fabrication of the given integrated circuit?
A. Photomask wearability
B. Number of simultaneously processing semiconductor wafers
C. Number of topological layers formed on the wafer
D. Minimum of feature size
E. Production volume

5a2. What semiconductor material has the maximum band gap?
A. Si
B. Ge
C. GaAs
D. SiC
E. The correct answer is missing

5a3. The performance of MOS transistor can be increased by:
A. Increasing the temperature
B. Decreasing the temperature
C. Changing the channel doping level
D. Decreasing thickness of dielectric layer
E. Increasing the gate voltage

5a4. Based on what semiconductor is it possible to make p-n junctions having higher operating temperatures?
A. Ge, Eg=0,66 eV
B. Si, Eg=1,12 eV
C. GaAs, Eg=1,45 eV
D. SiC, Eg= 3,1 eV
E. The correct answer is missing

5a5. The best resolution to form topological pattern provides
A. X-ray lithography
B. Electron beam lithography
C. Photolithography
D. Chemical lithography
E. All the answers are correct

5a6. What kind of P-N junction is it possible to produce by epitaxial technology?
A. Linearly graded P-N junction
B. P-N junction by exponent function
C. Abrupt P-N junction
D. All the answers are correct
E. The correct answer is missing

5a7. Operating frequency of bipolar transistors can be increased by
A. Increasing emitter effectiveness
B. Decreasing base width
C. Applying collector large voltages
D. Decreasing base impurity level
E. Increasing signal frequency

5a8. Charge capacitance is larger than diffusion
A. Because it does not depend on the frequency
B. In reverse-biased mode of *p-n junction,*
C. In forward-biased mode of p-n junction
D. Because it depends on the value of applied voltage
E. Because it depends on the value of current

5a9. p-n junction current in reverse-biased mode can be reduced by:
A. The reduction of the density of impurities

B. The reduction of temperature
C. The reduction of contact potentials' difference
D. The reduction of applied voltage
E. The size reduction of p and n regions

5a10. Which semiconductor will have higher concentration of intrinsic carriers in the given temperature, for example T=300K.
A. Ge, Eg=0,66 eV
B. Si, Eg=1,12 eV
C. GaAs, Eg=1,45 eV
D. SiC Eg= 3,1eV
E. All the answers are correct

5a11. Diffusion first step (drive in) realization provides:
A. High surface density and large diffusion depth of impurities
B. High surface density and small diffusion depth of impurities
C. Low surface density and large diffusion depth of impurities
D. Low surface density and small diffusion depth of impurities
E. Low surface density of impurities

5a12. In semiconductor crystals dislocations are classified as:
A. Schottky defects
B. Linear structural defects
C. Frenkel defects
D. Surface structural defects
E. Volume structural defects

5a13. Epitaxial growth technology of the layers allows receiving:
A. Linearly graded P-N junction
B. P-N junction by exponent function
C. Abrupt P-N junction
D. P-N junction by arbitrary function
E. P-N junction by quadratic function

5a14. Zone-melting method advantage of silicon monocrystal growth over Chokhralsi method is conditioned by:
A. Absence of quartz melting tube
B. Low level of thermal gradient
C. High speed of monocrystal growth
D. Low temperature of the process
E. Presence of inexpensive equipment

5a15. For a diffusion from the infinite source the diffusion depth x_j depends on diffusion time t by the following expression:
A. $x_j \sim t$
B. $x_j \sim t^{1/2}$
C. $x_j \sim t^2$
D. $x_j \sim t^3$
E. $x_j \sim exp(t)$

5a16. The saturation of drain current on the output characteristic of p-n junction FET is determined by:
A. Self-restriction effect if drain current increase
B. Velocity saturation of channel majority carriers caused by drain voltage
C. Density Impurities in the channel
D. A and B
E. All the answers are correct

5a17. What is diode's I-V characteristic linearity conditioned by:
A. Ohmic contacts of diode
B. Crystal structure of output material
C. Contact potential difference of p-n junction
D. Density of impurities in the base
E. Width of output material band gap

5a18. The oxide layer of the metal-oxide-semiconductor transistor is formed by the following method:
- *A. Chemical*
- *B. Ion implantation*
- *C. Epitaxial deposition*
- *D. Thermal oxidation*
- *E. Diffusion*

5a19. When the diode is forward biased, which carriers create current?
- *A. Ions of impurity atoms*
- *B. Surface charges*
- *C. Majority carriers*
- *D. Minority carriers*
- *E. Free electrons of the base*

5a20. The temperature of diffusion process in silicon IC technology is
- *A. Less than 800^0C*
- *B. higher than 1500^0C*
- *C. In 1100…1300^0C range*
- *D. Independent of temperature*
- *E. All the answers are correct*

5a21. The current-voltage characteristic of the P-N junction
- *A. Is linear*
- *B. Is strictly non linear*
- *C. Forward current value smaller than reverse current*
- *D. Reverse current value higher than forward current*
- *E. Independent of temperature*

5a22. In case of which connection does the bipolar transistor provide simultaneous amplification of current, voltage and power?
- *A. Common collector*
- *B. Common base*
- *C. Common emitter*
- *D. When the transistor is used by separated base*
- *E. When emitter and base are short connected*

5a23. What is the load resistance of bipolar transistor look like connected by common base?
- *A. Larger than the resistance of collector p-n junction*
- *B. Smaller than the resistance of collector p-n junction*
- *C. Larger than the resistance of emitter p-n junction*
- *D. Equal to base resistance*
- *E. Equal to the resistance of input contact*

5a24. For an intrinsic semiconductor the electron concentration is 10^{14} cm^{-3}. What is the hole concentration?
- *A. Higher than 10^{14} cm^{-3}*
- *B. Less than 10^{14} cm^{-3}*
- *C. Equal to electron concentration*
- *D. All the answers are correct*
- *E. All the answers are wrong*

5a25. Semiconductor structures of A_3B_5 (GaAs, InP, InAs, GaSb) type are made by:
- *A. Heteroepitaxal growth method*
- *B. Diffusion method*
- *C. Homoepitaxal growth method*
- *D. Ion Implantation method*
- *E. Vacuum deposition method*

5a26. The speed of silicon thermal oxidation is limited by:
- *A. Speed of surface adsorption of oxidants (O_2, H_2O)*
- *B. Speed of diffusion oxidants through the SiO_2 layer to Si-SiO_2 interface*
- *C. Speed of oxidation reaction with silicon*
- *D. Speed of diffusion of gas results of silicon surface reaction*

E. All the answers are correct

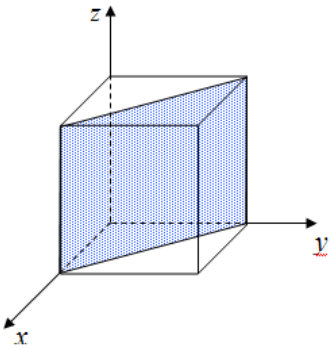
5a27. Thickness of silicon dioxide d is dependent on duration t of high-temperature oxidation by the following expression:

A. $d \sim t^{1/2}$
B. $d \sim t$
C. $d \sim t^2$
D. $d \sim t^3$
E. $d \sim \exp(t)$

5a28. What is the technology roadmap of photolithography process?

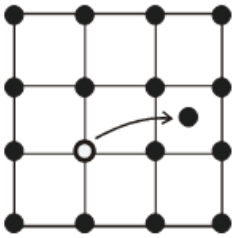
B. Photoresist Coating - alignment - development - exposure - etching
C. Photoresist Coating - development - alignment - exposure - etching
D. Photoresist Coating - alignment - exposure - etching - development
E. Photoresist Coating - exposure - alignment - etching - development
E.Photoresist Coating - alignment - exposure - development - etching

5a29. What crystal plane is shaded in cubic crystal?



A. (001)
B. (100)
C. (101)
D. (110)
E. (111)

5a30. What structural defect is figured?



A. Shottky defect
B. Linear structural defect
C. Frenkel defect
D. Surface structural defect
E. Volume structural defect.

5a31. Sub-collector n+ buried layer in n-p-n bipolar transistor structures is intended for:

A. Reducing the bulk resistance of lateral collector
B. Increasing the bulk resistance of lateral collector
C. Increasing the transient resistance of collector-emitter
D. Reducing the transient resistance of collector-emitter
E. Reducing the minority-carrier lifetime in collector

5a32. To obtain n-type semiconductor silicon in microelectronic processing the following are used as an impurity:

A. the elements of fifth group of periodic table
B. the elements of forth group of periodic table
C. the elements of third group of periodic table

D. the elements of first group of periodic table
E. the elements of sixth group of periodic table

5a33. To obtain p-type semiconductor silicon in microelectronic processing the following are used as an impurity:
A. the elements of forth group of periodic table
B. the elements of sixth group of periodic table
C the elements of third group of periodic table
D. the elements of fifth group of periodic table
E. the elements of second group of periodic table

5a34. In integrated circuit technology the photolithographic process is meant for:
A. forming the picture of topological layer on the substrate surface
B. getting thin metallic films on the substrate surface
C. getting thin dielectric films on the substrate surface
D. getting thick oxide films on the substrate surface
E. getting thin metallic and dielectric films on the substrate surface

5a35. In bipolar semiconductor integrated circuits the electric coupling between layers of the multilevel metalization is realized:
A. by diffusion structures
B. by metallic through holes
C. the electric coupling between layers is absent
D. by external metallic conductors
E .the correct answer is missing

5a36. In bipolar semiconductor integrated circuits the resistors are formed:
A .in terms of base region
B. in terms of emitter region
C. in terms of base- emitter junction
D. A and B answers are correct
E. A, B and C answers are correct

5a37. The design rules for integrated circuits
A. are used to design applications specific integrated circuits
B. define the minimal sizes of the elements and spacing between them during layout design
C. are non dependent on level of manufacturing process
D. are created by designer using design expertise
E. the correct answer is missing

5a38. In real p-n junctions beyond the defined value of the reverse voltage the reverse current:
A. sharply decreases
B. slowly decreases
C. sharply rises
D. slowly rises
E. remains practically constant

5a39. In semiconductor integrated circuits to form the doped regions with required type and conductance in the substrate the following methods are used:
A. diffusion and ion implantation
B. ion implantation and thermal oxidation
C. ion etching and diffusion
D. diffusion and thermal oxidation
E. the correct answer is missing

b) Problems

5b1.

For a silicon p-n junction the specific resistances of p and n-regions are 10^{-4} Ohm·m and 10^{-2} Ohm·m correspondingly. Calculate the contact potential of the junction at a room temperature when T=300K if the mobility of holes and electrons are 0,05 $m^2 V^{-1} s^{-1}$ and 0,13 $m^2 V^{-1} s^{-1}$. The intrinsic concentration at a room temperature equals $1{,}38 \times 10^{16} m^{-3}$.

5b2.
Calculate the density of electrons and holes in a p-Ge at a room temperature if the sample specific conductance equals 100 S/cm, mobility of holes is 1900 $cm^2 V^{-1} s^{-1}$, and $n_i=2{,}5x10^{13}$ atom/cm^3.

5b3.
The silicon sample is doped with a donor impurity $N_d= 10^{17}$atom/cm^3. The sample length equals 100μm, width 10 μm, and thickness 1 μm. Calculate the resistance and sheet resistance.

5b4.
What thickness of SiO_2 layer is required to fabricate a MOS capacitor with a specific capacity of 100nF/cm^2 (ε_{SiO2}=3,8x8,85x10^{-14} F/cm).
What oxidation process (wet or dry) would be used to grow the gate high quality oxide?

5b5.
The gate capacitance of the MOS transistor equals C. The capacitor structure is scaled by the factor α =2 . How will the gate capacitance change?

5b6.
Semiconductor's band gap width Eg = 0.7eV and the temperature does not change when T_1 = 250 K changes to T_2 = 300 K. V=0.4V forward bias voltage is applied to the p-n junction created in it. Define $\frac{j_2}{j_1}$ change of current density in the mentioned range of temperature change if in case of T_2 = 300 K, kT = 0.026eV.

5b7.
How will the channel of p-n junction field effect transistor change when the drain voltage is V=+0.1 V, if the dielectric transparency of semiconductor ε = 12, and for vacuum $\varepsilon_0 = 8.86 \cdot 10^{-12}$ F/m, contact difference of potentials φ_k=0.6V, electron charge $q=1.6*10^{19}$ K, and donor density in n channel $N_d=10^{15}$ cm^{-3}. Ignore the effects of source-drain and gate-drain domains.

5b8.
Calculate the drain current of a silicon n-MOSFET for the following conditions: V_t = 1 V, gate width W = 10 μm, gate length L = 1μm and oxide thickness t_{ox} = 10 nm. The device is biased with V_{GS} = 3 V and V_{DS} = 5 V. Use the device quadratic model, a surface mobility of 300 cm^2/V-s and V_{BS} = 0 V.

5b9.
For a silicon n-channel MOS FET the source- drain distance is 1μm and the doping levels are N_d =10^{20} cm^{-3}. The substrate doping is $N_a = 10^{16}$ cm^{-3}. Assume that the source and substrate are grounded. At what V_D voltage on the drain the deplation widths of the source and drain p-n junctions will meet (punch-through effect).

5b10.
The donor impurity concentration in the silicon substrate is changed by the linear law N=kx [cm^{-3}], where k= 8 x 10^{18} cm^{-4} and x is a distance. Calculate the electrons diffusion current density, when the electric field is absent. The electrons mobility at room temperature (T=300 K) is 1200 cm^2/V·s.

5b11.
For the silicon n^+ - p - n bipolar transistor the base width is W_B=0,6um, the doping levels of emitter, collector and base are N_{de} =10^{19} cm^{-3}, N_{dc} =5x10^{16} cm^{-3} and N_{ab}=5x10^{15} cm^{-3}
respectively. Define the collector critical voltage, when the device becomes uncontrolled (punch-through in the base region). Assume that T=300 K and intrinsic concentration is n_i=1,5x10^{10} cm^{-3}.

6. NUMERICAL METHODS AND OPTIMIZATION

a) Test questions

6a1. Fragmentation consecutive algorithm, compared with iteration algorithm, has:

A. More accuracy
B. Higher performance
C. Less accuracy
D. More machine time
E. B and C together

6a2. Which is the inverse polynomial of X^4+X+1?

A. X^3+X+1
B. X^4+X+1
C. X^4+X^2+1
D. X^4+X^3+1
E. The correct answer is missing

6a3. Which of the given intrinsic description forms more accurately describes an electrical circuit?

A. The graph of commutation schema
B. Complex list
C. Adjacency matrix
D. A and B equally
E. B and C equally

6a4. The following problem of linear programming is:

$$2x_1 + 3x_2 \to \max$$
$$\begin{cases} 7x_1 + 6x_2 \le 42 \\ -x_1 + 5x_2 \le 15 \\ x_1 \ge 0,\ x_2 \ge 0: \end{cases}$$

A. Does not have solution
B. One solution
C. Two solutions
D. Solutions with infinite set
E. Has unlimited solutions

6a5. In case of which values of parameter λ the following problem has infinite set of solutions?

$$f(X) = \lambda x_1 + x_2 \to \min_{X \in D},$$
$$D: \begin{cases} x_1 + 2x_2 \ge 2, \\ x_1 - 4x_2 \le 2, \\ 6x_1 + 5x_2 \le 30, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. 2
B. 1/2
C. 1
D. 1/4
E. 1/8

6a6. In case of which values of λ_1,λ_2 parameters the following problem has one solution?

$$f(X) = \lambda_1 x_1 + \lambda_2 x_2 \to \min_{X \in D},$$
$$D: \begin{cases} x_1 + 2x_2 \ge 2, \\ x_1 - 4x_2 \le 2, \\ 6x_1 + 5x_2 \le 30, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. $\lambda_1 = 1, \lambda_2 = 4,$

B. $\lambda_1 = 1/\ 2, \lambda_2 = 1,$

C. $\lambda_1 = 2, \lambda_2 = 4,$

D. $\lambda_1 = 4, \lambda_2 = 8,$

E. $\lambda_1 = 1, \lambda_2 = 2,$

6a7. In case of what values of λ parameters the following problem does not have a solution?

$$f(X) = x_1 + x_2 + x_3 \to \max_{X \in D},$$

$$D : \begin{cases} x_1 + x_3 = 2, \\ x_1 + 2\lambda x_2 + x_3 = 0, \\ x_1 \geq 0, x_2 \geq 0, x_3 > 0: \end{cases}$$

A. 0,
B. 5,
C. 1,
D. 1/2,
E. 2

6a8. In case of what values of b_{21} and b_{22} elements

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 0 & 1 & 2 \\ 4 & 2 & 0 \end{bmatrix}, \ B = \begin{bmatrix} 1 & 2 \\ b_{21} & b_{22} \\ 0 & 1 \end{bmatrix}$$

matrix system will not be fully controllable?

A. $b_{21} \neq 0, b_{22} = 0,$
B. $b_{21} = 0, b_{22} = 0,$
C. $b_{21} \neq 0, b_{22} \neq 0,$
D. $b_{21} = 0, b_{22} \neq 0,$
E. The correct answer is missing

6a9. In case of which values of b_{11} and b_{12} elements

$$A = \begin{bmatrix} 1 & 0 & 2 \\ 2 & 1 & 0 \\ 0 & 2 & 4 \end{bmatrix}, \ B = \begin{bmatrix} b_{11} & b_{12} \\ 1 & 2 \\ 2 & 0 \end{bmatrix}$$

matrix system will not be fully controllable?

A. $b_{11} = 0, b_{12} = 0,$
B. $b_{11} = 1, b_{12} = 2,$
C. $b_{11} = 2, b_{12} = 0,$
D. $b_{11} = 1, b_{12} = 0,$
E. $b_{11} = 0, b_{12} = 1,$

6a10. In case of which values of c_{11} and c_{12} elements

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 1 & 2 & 0 \\ 1 & 1 & 1 \end{bmatrix}, \ C = \begin{bmatrix} c_{11} & c_{12} & 0 \\ 1 & 2 & 3 \end{bmatrix}$$

matrix system will not be fully observable?

A. $c_{11} = 0, c_{12} = 0,$
B. $c_{11} \neq 0, c_{12} = 0,$
C. $c_{11} = 0, c_{12} \neq 0,$
D. $c_{11} \neq 0, c_{12} \neq 0,$
E. The correct answer is missing

6a11. In case of what values of b_{11}, b_{21} and b_{31} elements

$$A=\begin{bmatrix}2 & 1 & 0\\ 1 & 2 & 1\\ 2 & 1 & 1\end{bmatrix},\ B=\begin{bmatrix}b_{11} & 0\\ b_{21} & 2\\ b_{31} & 1\end{bmatrix}$$

matrix system will not be normal system?

A. $b_{11}=0,\ b_{21}=0,\ b_{31}=0,$
B. $b_{11}=0,\ b_{21}\neq 0,\ b_{31}=1,$
C. $b_{11}\neq 0,\ b_{21}=0,\ b_{31}=2,$
D. $b_{11}=1,\ b_{21}=1,\ b_{31}=1,$
E. $b_{11}=2,\ b_{21}\neq 1,\ b_{31}=0,$

6a12. For the given game model: at which values of p and q the expression $(i_0,j_0)=(2,2)$ is the best strategy?

$$\begin{bmatrix}1 & q & 6\\ p & 5 & 10\\ 6 & 2 & 3\end{bmatrix}$$

A. $p\leq 5$ *and* $q\geq 5$
B. $p\leq 5$ *and* $q\leq 5$
C. $p\geq 5$ *and* $q\leq 5$
D. $p\geq 5$ *and* $q\geq 5$
E. The correct answer is missing

6a13. For the given game model, in case of which values of n and m $(i_0,j_0)=(2,2)$ will be the best strategy?

$$\begin{bmatrix}0 & m & 5\\ n & 4 & 9\\ 5 & 1 & 2\end{bmatrix}$$

A. $n\leq 4$ *and* $m\geq 4$
B. $n\leq 4$ *and* $m\leq 4$
C. $n\geq 4$ *and* $m\leq 4$
D. $n\geq 4$ *and* $m\geq 4$
E. The correct answer is missing

6a14. For the given game model, in case of which values of p and q $(i_0,j_0)=(2,2)$ will be the best strategy?

$$\begin{bmatrix}4 & 6 & 3\\ 15 & 11 & q\\ 2 & p & 9\end{bmatrix}$$

A. $p\geq 11$ *and* $q\leq 11$
B. $p\leq 11$ *and* $q\leq 11$
C. $p\geq 11$ *and* $q\geq 11$
D. $p\leq 11$ *and* $q\geq 11$
E. The correct answer is missing

6a15. For the given game model, in case of which values of n and m, $(i_0,j_0)=(2,2)$ will be the best strategy?

$$\begin{bmatrix} 5 & m & 10 \\ n & 8 & 14 \\ 10 & 6 & 7 \end{bmatrix}$$

A. $n \le 8$ *and* $m \ge 8$
B. $n \le 8$ *and* $m \le 8$
C. $n \ge 8$ *and* $m \le 8$
D. $n \ge 8$ *and* $m \ge 8$
E. The correct answer is missing

6a16. What is the form of $u_{1opt}(t)$ -Ý, $u_{2opt}(t)$ if

$$I = \int_0^T u_2^2(t)dt \to \min_{u_1(t),u_2(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 1 & 2 \\ 0 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{bmatrix} 0 & 1 \\ 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix},$$

$$c(u_1(t),u_2(t)) = u_1^2(t) + u_2^3(t) \le 0,$$

whereas $\psi_1(t)$ and $\psi_2(t)$ are conjugated variables, and μ - is a special multiplier .

A. $u_{1opt}(t) = -\frac{1}{2} \cdot \frac{\psi_2(t)}{\mu}$, $u_{2opt}(t) = \frac{1 \pm \sqrt{1+12(\psi_1(t)+\psi_2(t))}}{6\mu}$

B. $u_{1opt}(t) = \psi_1(t) + \psi_2(t)$, $u_{2opt}(t) = \frac{1}{2\mu}(\psi_1(t) - \psi_2(t))$

C. $u_{1opt}(t) = \frac{\psi_1(t)}{\mu}$, $u_{2opt}(t) = \psi_1(t) \cdot \psi_2(t)$

D. $u_{1opt}(t) = \psi_1(t)$, $u_{2opt}(t) = \frac{\psi_1(t)}{\psi_2(t)} \cdot \mu$

E. The correct answer is missing

6a17. Which is the system of complement variables if

$$I = \int_0^T u^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 1 \\ 2 \end{pmatrix} \cdot u(t).$$

A. $\dot{\psi}_1(t) = -\psi_1(t) + \psi_2(t)$, $\dot{\psi}_2(t) = \psi_1(t) - \psi_2(t)$

B. $\dot{\psi}_1(t) = \psi_1(t) \cdot \psi_2(t)$, $\dot{\psi}_2(t) = \frac{\psi_1(t)}{\psi_2(t)}$

C. $\dot{\psi}_1(t) = -\psi_1(t) \cdot \psi_2(t)$, $\dot{\psi}_2(t) = -\frac{\psi_1(t)}{\psi_2(t)}$

D. $\dot{\psi}_1(t) = -2 \cdot \psi_1(t) - \psi_2(t)$, $\dot{\psi}_2(t) = -\psi_1(t) - 2 \cdot \psi_2(t)$

E. The correct answer is missing

6a18. What is the form of $u_{opt}(t)$ if

$$I = \int_0^T x_1^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 2 & 2 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 0 \\ 1 \end{pmatrix} \cdot u^2(t),$$

$$c(x_1(t)) = x_1^2(t) + x_1(t) \le 0,$$

whereas $\psi_1(t)$ and $\psi_2(t)$ are conjugated variables, and μ - is a special multiplier .

A. $u_{opt}(t) = \dfrac{\psi_1(t)}{\mu + \psi_2(t)}$

B. $u_{opt}(t) = \dfrac{\psi_2(t)}{\mu + \psi_1(t)}$

C. $u_{opt}(t) = \psi_1(t) + \dfrac{\psi_2(t)}{\mu}$

D. $u_{opt}(t) = -2 \cdot (1 + 2x_1(t)) \cdot \dfrac{\mu}{\psi_2(t)}$

E. The correct answer is missing

6a19. What category is

$$c(x_1(t)) = x_1^2(t) + x_1(t) \le 0$$

limitation if

$$I = \int_0^T x_1^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 2 & 2 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 0 \\ 1 \end{pmatrix} \cdot u^2(t).$$

A. 1st category
B. 2nd category
C. 3rd category
D. 4th category
E. 7th category

6a20. If j^{th} component of optimal solution of dual canonic problem of linear programming equals zero ($y_j=0$), then direct problem's appropriate limitation is.

A. > 0
B. < 0
C. $= 0$
D. ≥ 0
E. The correct answer is missing

6a21. If j^{th} component of optimal solution of dual canonic problem of linear programming doesn't equal zero ($y_j \ne 0$), then direct problem's appropriate limitation is.

A. $> 0,$
B. $= 0,$
C. $< 0,$
D. $= 8,$
E. The correct answer is missing

6a22. For the solution of canonic problem of linear programming which condition must take place (n is the number of variables of direct problem, and m is the number of limitations).

A. $x_i^{direct} = -(sd)_{m+i}^{dual}$
B. $x_i^{direct} = (sd)_{n+i}^{dual}$

C. $x_i^{direct} = -(sd)_{n+i}^{dual}$

D. $x_i^{direct} = (sd)_{m+i}^{dual}$

E. The correct answer is missing

6a23. Which condition is valid for the optimal solution of canonical problems of linear programming (n-is the number of variables of direct problem and m-is the number of limitations).

A. $y_i^{dual} = (sd)_{n+i}^{direct}$

B. $y_i^{dual} = -(sd)_{n+i}^{direct}$

C. $y_i^{dual} = -(sd)_{m+i}^{direct}$

D. $y_i^{dual} = (sd)_{m+i}^{direct}$

E. The correct answer is missing

6a24. In case of which value of a_{33} cell

$$A = \begin{bmatrix} 1 & 0 & 0 \\ 2 & 2 & 4 \\ 1 & 0 & a_{33} \end{bmatrix}$$

matrix can be reduced to diagonal form?

A. $a_{33} = 1,$

B. $a_{33} = 2,$

C. $a_{33} \neq 1,$

D. $a_{33} \neq 1$ *or* $a_{33} \neq 2,$

E. The correct answer is missing

6a25. P_2 coefficient of characteristic polynomial

$$P_0 \cdot \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0$$

of the following matrix

$$A = \begin{bmatrix} 2 & 0 & 0 \\ 1 & 1 & 2 \\ 1 & 0 & 3 \end{bmatrix}$$

equals

A. +11,

B. 6,

C. -11,

D. 0,

E. -6

6a26. What does $\Psi^T(t) \cdot \Psi(t)_{|t=2}$ equal if it is known that

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 0 & -1 & 2 \\ 1 & 0 & 3 \\ -2 & -3 & 0 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix}, \quad \begin{matrix} x_1(0) = 1, \\ x_2(0) = 2, \\ x_3(0) = 0, \end{matrix}$$

and $\Psi(t) = (\psi_1(t), \psi_2(t), \psi_3(t))^T$ is complement variable vector

A. -5

B. -3

C. 0

D. 3

E. 5

6a27. What does $X^T(t)\cdot X(t)_{|t=3}$ equal if it is known that

$$\begin{pmatrix}\dot{\psi}_1(t)\\ \dot{\psi}_2(t)\\ \dot{\psi}_3(t)\end{pmatrix}=\begin{bmatrix}0 & 2 & -1\\ -2 & 0 & 1\\ 1 & -1 & 0\end{bmatrix}\cdot\begin{pmatrix}\psi_1(t)\\ \psi_2(t)\\ \psi_3(t)\end{pmatrix},\ \begin{matrix}\psi_1(0)=2,\\ \psi_2(0)=1,\\ \psi_3(0)=3,\end{matrix}$$

and $X(t)=(x_1(t),x_2(t),x_3(t))^T$ is the variable vector of the state.

A. 6
B. 8
C. 11
D. 14
E. 17

6a28. The reminder of the division of the polynomial $15x^4-14x^3+8x^2-7x-2$ by the binomial $x-1$ is

A. 3
B. 4
C. 0
D. -8
E. -2

6a29. What point belongs to the graph of the function $f(x)=3x^4-2x+1$?

A. (5,-1)
B. (0,3)
C. (-1,6)
D. (1,4)
E. (-2,-1)

6a30. What value does the derivative of the function $f(x)=x(x-1)(x-2)(x-3)(x-4)(x-5)$ have in the point $x=0$?

A. -200
B. -120
C. -50
D. 100
E. 150

6a31. What number is the eigenvalue of the matrix $A=\begin{pmatrix}5 & 1\\ 2 & 4\end{pmatrix}$?

A. 5
B. 2
C. -1
D. 3
E. 8

6a32. For what value of α parameter $M=\begin{pmatrix}3 & 7 & 1\\ 2 & -3 & 0\\ 1 & \alpha & 1\end{pmatrix}$ matrix does not have inverse?

A. 3
B. 0
C. -2
D. 10
E. 15

6a33. For what value of A parameter $f(x)=\begin{cases}\dfrac{\sin 3x}{x}, x\neq 0\\ A, x=0\end{cases}$ function will be continuous?

A. 0

B. 1
C. -1
D. 4
E. 3

6a34. Arrange the following integrals in ascending order.

$$I_1 = \int_1^2 \frac{dx}{\sqrt{x}+1} \qquad I_2 = \int_1^2 \frac{2\sin x}{\sqrt[3]{x}}dx \qquad I_3 = \int_1^2 \frac{dx}{x+e^x}$$

A. I_3, I_1, I_2
B. I_2, I_3, I_1
C. I_1, I_2, I_3
D. I_2, I_1, I_3
E. I_1, I_3, I_2

6a35. How many real roots does $f'(x)=0$ equation have where $f(x)=(x-1)(x-2)(x-3)(x-4)(x-5)$

A. 4
B. 3
C. 2
D. 1
E. 0

6a36. For what value of a_{22} element

$$A=\begin{bmatrix} 2 & 0 & 0 \\ 1 & a_{22} & 0 \\ 2 & 1 & 1 \end{bmatrix}$$

matrix can be reduced to diagonal form?

A. $a_{22}=2$
B. $a_{22}=1,$
C. $a_{22}\neq 1,$
D. $a_{22}\neq 2$ *and* $a_{22}\neq 1$
E. The correct answer is missing

6a37. For what values of c_{11} and c_{21} elements

$$A=\begin{bmatrix} 3 & 0 & 0 \\ 0 & 2 & 0 \\ 0 & 0 & 1 \end{bmatrix},\ C=\begin{bmatrix} c_{11} & 1 & 0 \\ c_{21} & 1 & 2 \end{bmatrix}$$

Matrix system will not be fully observable?

A. $c_{11}\neq 0,\ c_{21}=0$
B. $c_{11}=0,\ c_{21}=0$
C. $c_{11}=0,\ c_{21}\neq 0$
D. $c_{11}\neq 0,\ c_{21}\neq 0$
E. The correct answer is missing

6a38. What category is

$$c(x_1(t)) = x_1^2(t) + x_1(t) \leq 0$$

limitation if

$$I = \int_0^T x_1^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 0 \\ 2 \end{pmatrix} \cdot u^3(t).$$

A. 1st category
B. 3rd category
C. 4th category
D. 2nd category
E. 5th category

6a39. For what values of b_{31} and b_{32} elements

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 1 & 2 & 0 \\ 0 & 1 & 3 \end{bmatrix}, \; B = \begin{bmatrix} 1 & 2 \\ 2 & 0 \\ b_{31} & b_{32} \end{bmatrix}$$

matrix system will not be fully controllable?
A. $b_{31}=1$, $b_{32}=2$,
B. $b_{31}=2$, $b_{32}=0$,
C. $b_{31}=0$, $b_{32}=0$,
D. $b_{31}=1$, $b_{32}=0$,
E. $b_{31}=0$, $b_{32}=1$,

6a40. What is the view of $u_{1opt}(t)$, $u_{2opt}(t)$ if

$$I = \int_0^T (u_1^2(t) + u_2^2(t))dt \to \min_{u_1(t),u_2(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix},$$

A. $u_{1opt}(t) = \psi_1(t) + \psi_2(t), \; u_{2opt}(t) = \psi_1(t) - \psi_2(t),$

B. $u_{1opt}(t) = \psi_1(t) \cdot \psi_2(t)$, $u_{2opt}(t) = \dfrac{\psi_1(t)}{\psi_2(t)},$

C. $u_{1opt}(t) = \dfrac{\psi_2(t)}{\psi_1(t)}, \; u_{2opt}(t) = 0,$

D. $u_{1opt}(t) = \dfrac{1}{2}(\psi_1(t) + \psi_2(t)), \; u_{2opt}(t) = \dfrac{1}{2}\psi_2(t),$

E. The correct answer is missing:

6a41. Which statement is right?
A. Direct and dual problems have the same number of variables
B. The objective functions of direct and dual problems have the same value
C. Direct and dual problems have the same number of limitations
D. None
E. All the answers are correct

6a42. For what value of a_{22} element

$$A = \begin{bmatrix} 2 & 0 & 0 \\ 2 & a_{22} & 0 \\ 2 & 2 & 1 \end{bmatrix}$$

matrix can be reduced to diagonal form?
A. $a_{22} = 2$

B. $a_{22}=1$

C. $a_{22}\neq 1$

D. $a_{22}\neq 2$ *or* $a_{22}\neq 1$

E. The correct answer is missing

6a43. For what values of c_{11} and c_{21} elements

$$A=\begin{bmatrix}1 & 0 & 0\\ 0 & 2 & 0\\ 0 & 0 & 3\end{bmatrix},\ C=\begin{bmatrix}c_{11} & 2 & 0\\ c_{21} & 3 & 2\end{bmatrix}$$

matrix system will not be fully observable?

A. $c_{11}\neq 0,\ c_{21}=0$

B. $c_{11}=0,\ c_{21}=0$

C. $c_{11}=0,\ c_{21}\neq 0$

D. $c_{11}\neq 0,\ c_{21}\neq 0$

E. The correct answer is missing

6a44. What is $X^{T}(t)\cdot X(t)_{|t=3}$ equal to, if it is known that

$$\begin{pmatrix}\dot{\psi}_1(t)\\ \dot{\psi}_2(t)\\ \dot{\psi}_3(t)\end{pmatrix}=\begin{bmatrix}0 & 2 & -1\\ -2 & 0 & 1\\ 1 & -1 & 0\end{bmatrix}\cdot\begin{pmatrix}\psi_1(t)\\ \psi_2(t)\\ \psi_3(t)\end{pmatrix},\ \begin{matrix}\psi_1(0)=0,\\ \psi_2(0)=1,\\ \psi_3(0)=3,\end{matrix}$$

and $X(t)=(x_1(t),x_2(t),x_3(t))^{T}$ is conjugate variable vector.

A. 0

B. 2

C. 6

D. 10

E. 14

6a45. Which is the conjugate variable system if

$$I=\int_0^T u^2(t)dt\to\min_{u(t)},$$

$$\begin{pmatrix}\dot{x}_1(t)\\ \dot{x}_2(t)\end{pmatrix}=\begin{bmatrix}1 & 3\\ 3 & 1\end{bmatrix}\cdot\begin{pmatrix}x_1(t)\\ x_2(t)\end{pmatrix}+\begin{pmatrix}2\\ 1\end{pmatrix}\cdot u(t).$$

A. $\dot{\psi}_1(t)=-\psi_1(t)-3\psi_2(t),\ \dot{\psi}_2(t)=-3\psi_1(t)-\psi_2(t)$

B. $\dot{\psi}_1(t)=-\psi_1(t)+\psi_2(t),\ \dot{\psi}_2(t)=\psi_1(t)-\psi_2(t)$

C. $\dot{\psi}_1(t)=\psi_1(t)\cdot\psi_2(t),\ \dot{\psi}_2(t)=\dfrac{\psi_1(t)}{\psi_2(t)}$

D. $\dot{\psi}_1(t)=-\dfrac{\psi_2(t)}{\psi_1(t)},\ \dot{\psi}_2(t)=\psi_1(t)\cdot\psi_2(t)$

E. The correct answer is missing

6a46. What does $\Psi^{T}(t)\cdot\Psi(t)_{|t=2}$ equal if it is known that

$$\begin{pmatrix}\dot{x}_1(t)\\ \dot{x}_2(t)\\ \dot{x}_3(t)\end{pmatrix}=\begin{bmatrix}0 & 1 & -1\\ -1 & 0 & 2\\ 1 & -2 & 0\end{bmatrix}\cdot\begin{pmatrix}x_1(t)\\ x_2(t)\\ x_3(t)\end{pmatrix},\ \begin{matrix}x_1(0)=1,\\ x_2(0)=2,\\ x_3(0)=-3,\end{matrix}$$

and $\Psi(t)=(\psi_1(t),\psi_2(t),\psi_3(t))^{T}$ is the conjugate variable vector.

A. 14

B. 10

C. 6
D. 2
E. 0

6a47. P_3 coefficient of characteristic polynomial

$$\boldsymbol{P_0 \cdot \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0}$$

of the following matrix

$$A = \begin{bmatrix} 1 & 0 & 0 \\ 2 & 3 & 1 \\ 2 & 0 & 4 \end{bmatrix}$$

equals

A. 12
B. 5
C. 4
D. 3
E. 1

6a48. For which values of $\boldsymbol{b_{11}}$, $\boldsymbol{b_{21}}$ and $\boldsymbol{b_{31}}$ elements

$$A = \begin{bmatrix} 1 & 2 & 0 \\ 2 & 1 & 1 \\ 1 & 1 & 2 \end{bmatrix},\ B = \begin{bmatrix} b_{11} & 1 \\ b_{21} & 2 \\ b_{31} & 3 \end{bmatrix}$$

matrix system will not be normal system.
A. $b_{11}\neq 0$, $b_{21}=0$, $b_{31}\neq 0$
B. $b_{11}=0$, $b_{21}=0$, $b_{31}\neq 0$
C. $b_{11}=0$, $b_{21}=0$, $b_{31}=0$
D. $b_{11}=1$, $b_{21}=0$, $b_{31}=2$
E. $b_{11}=2$, $b_{21}=1$, $b_{31}=0$

6a49. How many real roots has the equation $\frac{df}{dx}(x) = 0$ for the function $f(x) = x^6 - 6x^4 + x + 2$?

A. 0
B. 1
C. 2
D. 3
E. 4

6a49. Calculate the integral $\int_1^4 |x-2| dx$

A. 3
B. 2.5
C. 2
D. 1.5
E. 1

6a50. For which α the rank of matrix

$$A = \begin{pmatrix} \alpha & 1 & 1 \\ 1 & \alpha & 1 \\ 1 & 1 & \alpha \end{pmatrix}$$

is equal to 2?
A. -2
B. 0
C. 1
D. 3

E. All the answers are correct

6a51. How many significant digits of $\lg 2$ should be taken for determination of the roots of equation $x^2 - 2x + \lg 2 = 0$ with 4 digit accuracy?

A. 2
B. 4
C. 6
D. 8
E. 10

6a52. Assume $M = \begin{pmatrix} 2 & 4 \\ 1 & 2 \end{pmatrix}$. The equality $M^6 = kM$ holds if k is

A. 2^6
B. 2^8
C. 2^{10}
D. 2^{12}
E. 2^{14}

6a53. From the given points A, B, C, D which one is the closest to $y = 3x + 2$ line?

A. A(1,2)
B. B(3,2)
C. C(0,-1)
D. D(-1,-2)
E. C and D answers are correct

6a54. Find $\lim\limits_{n\to\infty} \sum\limits_{k=1}^{n} \dfrac{1}{n\left(1+\dfrac{k}{n}\right)}$

A. 1
B. ln2
C. 0.5
D. 0
E. The correct answer is missing

6a55. Assume $f(x) = e^x \cos 2x$. What second degree polynomial gives the best approximation of function f in the neighborhood of 0?

A. $P_2 = 1 + 0.2x + x^2$
B. $P_2 = 1 + x - 1.5x^2$
C. $P_2 = 1 - 2.5x + 3x^2$
D. $P_2 = 2 - x + 3x^2$
E. The correct answer is missing

6a56. Assume $f\left(x + \dfrac{1}{x}\right) = x^2 + \dfrac{1}{x^2}$ for all $x \neq 0$. In that case f function is defined by the following expression:

A. $x^2 - 2$
B. $2x^2 + 1$
C. $x^2 + 4$
D. $4x - x^2$
E. $3x + x^2 + 1$

6a57. For

$$f(x)=\begin{cases} e^x, & x>0 \\ a+x, & x\le 0 \end{cases}$$

function to be constant, a constant value must equal

A. 2,
B. 1
C. 0
D. -1
E. -2

6a58. What does $\lim_{n\to\infty} \sqrt[2n]{1+x^{2n}}$ limit equal?

A. $|x|+1$

B. $\min(2,|x|)$

C. $\max(1,|x|)$

D. 1

E. $2|x|$

6a59. In case of what β

$$\begin{cases} x_1+x_2+x_3=0 \\ x_1+\beta x_2+x_3=0 \\ x_1+x_2+2x_3=0 \end{cases}$$

system has more than three solutions?

A. 4,
B. 3,
C. 2,
D. 1
E. 0

6a60. Find $\lim_{n\to\infty} \int_0^{\infty} \frac{dx}{x^n+1}$ limit

A. 1,
B. 2,
C. 3,
D. 4
E. 5

6a61. Assume random value distribution function is given by $F(x)=A(B+arctg2x)$ formula. Define A and B constant values.

A. $A=1,\ B=0.5\pi$

B $A=\pi^{-1},\ B=0.5\pi$

C. $A=(2\pi)^{-1},\ B=\pi$

D. $A=\pi^{-1},\ B=1$

E. $A=2\pi^{-1},\ B=\pi$

6a62. Assume A matrix looks as follows:

$$A=\begin{pmatrix} 0.2 & 5 \\ \alpha & 0.1 \end{pmatrix}$$

what value of α of $\bar{x}=A\bar{x}$ system can be solved by sequential approximation method?

A. 2
B. 1

C. 0
D. -1
E. -2

6a63. Which of $A(3,5)$, $B(2,6)$, $C(-1,1)$, $D(2,0)$, $E(5,0)$ points is the nearest to $y = 3x + 1$?
A. A
B. B
C. C
D. D
E. E

b) Problems

6b1.
The following matrix game is given:

$$H = \begin{bmatrix} 3 & -2 & 4 \\ -1 & 4 & 2 \\ 2 & 2 & 6 \end{bmatrix}$$

Find the worth of game, optimal strategies and characterize the game. If necessary, construct corresponding problems of mathematical programming.

6b2.
Define the first two members of Taylor series $\Phi(t, t_0)$ if

$$A(t) = \begin{bmatrix} t & t^2 & t^3 \\ 1 & t & (2-t) \\ t^2 & t & 1 \end{bmatrix}, \quad t_0 = 2:$$

6b3.
Define $\Phi(t)$ if

$$A = \begin{bmatrix} 2 & 1 & 0 \\ 0 & 3 & 0 \\ 2 & 1 & 1 \end{bmatrix}.$$

6b4.
Reduce the system to diagonal form if

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 0 & 1 & 0 \\ 2 & 1 & 3 \end{bmatrix}:$$

6b5.
The following matrix is given:

$$A = \begin{bmatrix} 1 & -2 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

What is the constant term of characteristic polynomial equal to?

6b6.
The following matrix is given:

$$A = \begin{bmatrix} 1 & -2 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

What is $||A||_2$ norm equal to?

6b7.

What is the coefficient of A_{3X3} matrix's characteristic polynomial term containing λ^2, if

$$\lambda_1 = 1, \lambda_2 = 2, \lambda_3 = 3$$

are the eigenvalues of A_{3X3}.

6b8.

What equals A_{4X4} matrix's characteristic polynomial coefficient of the term which contains λ^2, if

$$\lambda_1 = 0, \lambda_2 = 1, \lambda_3 = 2, \lambda_4 = 3$$

are the eigenvalues of A_{4X4}.

6b9.
The table of *log x* function in [0,1000] interval is built by the help of linear interpolation. What *h* step should be selected for the error not to exceed 0.001? Consider cases of constant and variable steps (by dividing the interval into several subintervals). Estimate the minimum number of nodes which is necessary to provide the given accuracy.

6b10.
Using generalized trapezoid rule, calculate

$$\int_0^1 \frac{e^x}{x^2 + b^2} dx$$

integral with $O(h^2)$ accuracy (*h* is division step). How should this formula be applied to provide the same accuracy if $b<<1$?

6b11.
Apply quadrature formula for the calculation of the integral

$$\int_0^1 \frac{f(x)}{\sqrt{x}} dx$$

with 10^{-4} accuracy, providing $|f''(x)| \le 1$.

6b12.
Define the initial approximation domains of x_0 for which

$$x_{n+1} = \frac{x_n^3 + 1}{20}$$

iterations converge.

6b13.

$f(x)=\dfrac{5}{1+100x^2}$ function is replaced by $y=\alpha x+\beta$ linear function in segment $[-10,10]$. Define coefficients α and β to provide the smallest error. Can such α and β uniquely be found? If yes, find it; if no – consider possible cases.

6b14.

Construct an approximate formula (multiple-application rectangle rule) for the calculation of the integral $\int_1^\infty \dfrac{f(x)dx}{1+x^2}$ with $\varepsilon=0,01$ accuracy. The function f on interval $[1,\infty)$ is continuously differentiable and bounded.

6b15.

Continuously differentiable function f is given on $[a,b]$ segment and $a<x_1<x_2<b$. Find the polynomial P_3 of the third order so that in x_1 and x_2 points its and its derivative's values coincide with $f(x_1)$, $f(x_2)$ and $f'(x_1)$, $f'(x_2)$ values respectively. Is it possible to generalize the obtained formula for arbitrary number of points $a<x_1<\ldots<x_2<b$?

6b16.

Find the roots of the equation $x^4-10x+1=0$ with $\varepsilon=0,01$ accuracy. Choose the fastest algorithm.

6b17.

Assume

$$f(x)=\frac{1}{1+x}+\frac{1}{3-x}.$$

Find $g(x)=ax^2+bx+c$ quadratic function, which gives the best approximation for the function f in $[0,2]$ interval. Consider different cases.

6b18.

Assume

$$\Delta_n=\det\begin{pmatrix} 2 & 1 & 0 & 0 & \cdots & 0\\ 1 & 2 & 1 & 0 & \cdots & 0\\ 0 & 1 & 2 & 1 & \cdots & 0\\ 0 & 0 & 1 & 2 & \cdots & 0\\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots\\ 0 & 0 & 0 & 0 & \cdots & 2 \end{pmatrix}.$$

Calculate the limit $\lim\limits_{n\to\infty}\dfrac{\Delta_n}{n}$.

6b19.

The triangle ABC is given by the three vertices $A(x_1,y_1)$, $B(x_2,y_2)$, $C(x_3,y_3)$. How to check if the given point D with coordinates $D(x_0,y_0)$ lies in interior of that triangle? Describe the algorithm. Is it possible to generalize this algorithm for the case of

a) convex polygon

b) arbitrary polygon.

6b20.

x_j, $j=1,2$, and y_k, $k=0,\ldots,4$ real numbers are given. Find the forth degree polynomial P_4 in a way that

$$P_4^{(k)}(x_1)=y_k,\ k=0,1,2,3;\quad P_4(x_2)=y_4.$$

Generalize the result: find the n-th degree polynomial P_n so that

$$P_n^{(k)}(x_1) = y_k,\ k = 0,\ldots,m;\quad P_n^{(j)}(x_2) = y_{m+1+j},\ j = 0,\ldots,n-m-1.$$

6b21.
The following matrix is given:

$$\mathrm{A} = \begin{bmatrix} 1 & -3 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

What does the free term of characteristic polynomial equal?

6b22.
Given

$$\mathrm{A} = \begin{bmatrix} 1 & -3 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

matrix. What does $||A||_2$ norm equal?

6b23.
What does A_{3X3} matrix's characteristic polynomial coefficient of the term which contains λ equal if

$$\lambda_1 = 1, \lambda_2 = 4, \lambda_3 = 2.$$

6b24.
What does A_{4X4} matrix's characteristic polynomial coefficient of the term which contains λ^2 equal if

$$\lambda_1 = 4, \lambda_2 = 1, \lambda_3 = 2, \lambda_4 = 3.$$

6b25.
Find the n degree polynomial P_n which satisfies the following conditions:

$P_n^{(j)}(1) = y_j,\quad j = 0,1,2,\qquad P_n^{(k)}(0) = z_k,\quad k = 0,1$

Find the smallest n for which the Problem has a solution for arbitrary values y_j and z_k. For this n find the polynomial P_n in explicit form.

6b26.
On the segment $[-1,1]$ find the best uniform approximation polynomial of order one P_1 for $f(x) = x^3$ function, i.e. find P_1 polynomial for which the uniform norm $\|f - P_1\| = \max_{x\in[-1,1]} |f(x) - P_1(x)|$ is minimal.

6b27.
Find the eigenvalues of the matrix A which satisfies the condition $A^2 = 0$ (0 is zero matrix). What may be said about the eigenvalues of the matrix A which satisfies the condition $A^n = 0$ where n is a natural number. Justify the answer.

6b28.
Calculate $\ln 2$ with 0.001 accuracy, using $\ln(1+x) = \sum_{k=1}^{\infty} (-1)^{k+1} \frac{x^k}{k}$ series for $|x| < 1$. Find more optimal solution, i.e.a method of solution which requires the smallest number of summands of series.

6b29.
The following matrix is given

$$A = \begin{bmatrix} 2 & -6 & 0 \\ 0 & 2 & 4 \\ -2 & 0 & 2 \end{bmatrix}$$

What does the free term of characteristic polynomial equal?

6b30.

What does A_{4x4} matrix's characteristic polynomial coefficient of the term which contains λ^2 equal if $\lambda_1 = 2, \lambda_2 = 0.5, \lambda_3 = 1, \lambda_4 = 1.5$:

6b31.

Given the matrix of state variables of controlling system.

$$A = \begin{bmatrix} -2 & 0 \\ 1 & -1 \end{bmatrix}$$

Define $\Phi(t)$ fundamental matrix of replacement.

6b32.

Find out full controllability of the system described by the following equations.

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 0.5 & 0 & 1 \\ 0.5 & 0.5 & 0 \\ 0 & 0.5 & 0.5 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} + \begin{bmatrix} 0 & 0.5 \\ 0.5 & 0 \\ 0.5 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix},$$

7. DISCRETE MATHEMATICS AND THEORY OF COMBINATIONS

a) Test questions

7a1. The set is countable if it is
- *A. Finite*
- *B. Equivalent to some subset of finite set*
- *C. Equivalent to any subset of natural number set*
- *D. Equivalent to any infinite set*
- *E. Equivalent to any infinite subset of natural number set*

7a2. The graph includes Euler cycle if and only if
- *A. It is connected and the degrees of all nodes are even*
- *B. It is connected and the degrees of some nodes are odd*
- *C. The degrees of all nodes are even*
- *D. It is not connected and the degrees of some nodes are even*
- *E. It is connected and the degrees of all nodes are odd*

7a3. If for $f(x_1,\dots,x_i,\dots,x_n)$ Boolean function $\omega_i^f = 1$ (i=1,2,…,n), then it is
- *A. Constant 1 preserving function*
- *B. Linear function*
- *C. Self-dual function*
- *D. Monotone function*
- *E. Constant 0 preserving function*

7a4. If Boolean function is monotonous, then
- *A. Its short disjunctive normal form does not contain negation of variables*
- *B. It is not self-dual*
- *C. Its short disjunctive normal form does not coincide with its minimal disjunctive normal form*
- *D. it is also a threshold*
- *E. it is not a threshold*

7a6. In the given design styles in what sequence does the performance increase in case of other same parameters a) library; b) gate matrix; c) full custom; d) programmable matrix;
- *A. d - b - a - c*
- *B. a - b - c - d*
- *C. b - d - a - d*
- *D. c - a - b - d*
- *E. d - c - b - a*

7a7. Which of the presented description forms of electrical circuit is more convenient for the realization of sequential placing algorithm?
- *A. Graph of commutation schema*
- *B. Complex list*
- *C. Adjacency matrix*
- *D. A and B equally*
- *E. B and C equally*

7a8. In case of the presented design styles, in what order does the density of cells' placing increase? a) standard IC design; b) library design; c) gate matrix design; d) full custom design; e) programmable matrix design.
- *A. b - a - c - e - d*
- *B. a - b - c - d - e*
- *C. d - c - b - e - a*
- *D. a - d - b - c - e*
- *E. d - b - c - e - a*

7a9. The activity of x_3 argument of $(x_1 \vee x_2) \oplus (x_3 \vee x_4 x_5))$ function equals
- *A. 1/4*
- *B. 1/8*
- *C. 3/8*
- *D. 5/8*
- *E. 3/4*

7a10. If for f(x_1, … , x_n) Boolean function $\omega^{f}_{1,2,\ldots,n}$=1, then f is

A. Constant 0 function
B. Constant 1 function
C. Monotone function
D. Self-dual function
E. Linear function

7a11. The activity of $x_1(\bar{x}_2 \vee x_3(x_4 \vee x_5 \bar{x}_6))$ function's x_1 argument equals

A. 25/32
B. 27/32
C. 21/32
D. 13/16
E. 19/32

7a12. $x_1(\bar{x}_2 \vee x_3(x_4 \vee x_5 \bar{x}_6))$ function's norm equals

A. 11/64
B. 13/32
D. 17/64
D. 21/64
E. 23/64

7a13. $(x_1 \vee x_2) \oplus (x_3 \vee x_4 x_5))$ function's norm equals

A. 7/16
B. 9/16
C. 13/16
D. 11/16
E. 5/16

7a14. f(x_1, … , x_n) is dual if

A. $\exists(\alpha_1,\ldots,\alpha_n)\ \bar{f}(\bar{\alpha}_1,\ldots,\bar{\alpha}_n) = f(\alpha_1,\ldots,\alpha_n)$

B. $\forall(\alpha_1,\ldots,\alpha_n)\ \bar{f}(\bar{\alpha}_1,\ldots,\bar{\alpha}_n) = f(\alpha_1,\ldots,\alpha_n)$

C. $\exists(\alpha_1,\ldots,\alpha_n)\ \bar{f}(\bar{\alpha}_1,\ldots,\bar{\alpha}_n) = \bar{f}(\alpha_1,\ldots,\alpha_n)$

D. $\exists(\alpha_1,\ldots,\alpha_n)\ f(\bar{\alpha}_1,\ldots,\bar{\alpha}_n) = f(\alpha_1,\ldots,\alpha_n)$

E. $\forall(\alpha_1,\ldots,\alpha_n)\ f(\bar{\alpha}_1,\ldots,\bar{\alpha}_n) = f(\alpha_1,\ldots,\alpha_n)$

7a15. The activity of the combination of arguments x_3 and x_4 for the function $(x_1 x_2) \oplus (x_3 \vee x_4)x_5$ is equal to:

A. 1/4
B. 7/16
C. 3/4
D. 11/16
E. 1/8

7a16. If $f(x_1,\ldots,x_n)$ is threshold function

A. $\bar{f}(x_1,\ldots,x_n)$ *is not threshold function*

B. $f(\bar{x}_1,\ldots,\bar{x}_n)$ *is not threshold function*

C. $\bar{f}(\bar{x}_1,\ldots,\bar{x}_n)$ *is threshold function*

D. $x \oplus f(x_1,...,x_n)$ *is threshold function*

E. $x \oplus \bar{f}(x_1,...,x_n)$ *is threshold function*

7a17. Binary relation is the equivalence relation if it is
A. Transitive, symmetric but not reflexive
B. Not symmetric, reflexive and transitive
C. Symmetric, reflexive but not transitive
D. Reflexive, transitive and symmetric
E. Not symmetric, not reflexive and transitive

7a18. $(x_3 \vee x_2) \oplus (\bar{x}_1 \vee x_4 x_5))$ function's norm equals
A. 9/16
B. 11/16
C. 13/16
D. 7/16
E. 5/16

7a19. The activity of $(x_3 \vee x_2) \oplus (x_1 \vee x_4 x_5))$ function's x_3 argument equals
A. 1/4
B. 1/8
C. 3/8
D. 5/8
E. 1/2

7a20. How many connectivity component does the complementation of the graph which has 4-connected component have?
A. 1
B. 2
C. 3
D. 4.
E. The correct answer is missing

7a21. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le Û \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. Set T of input vectors is a test with respect to the set Φ of faults if
A. For any $f \in \Phi$ *and for any an input vector* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, *and for any* j, $1 \le j \le m$, $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \equiv f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;
B. For any $f \in \Phi$ *and for any input vector* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, *and for any* j, $1 \le j \le m$, $f_Û^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;
C. For any $f \in \Phi$ *there exists an input vector* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, *and there exists a* j, $1 \le j \le m$, *such that* $f_Û^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \le f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;
D. For any $f \in \Phi$ *there exists such an input vector* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, *and there exists a* j, $1 \le j \le m$, *such that* $f_Û^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ge f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$.
E. For any $f \in \Phi$ *there exists an input vector* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, *and there exists a* j, $1 \le j \le m$, *such that* $f_Û^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

7a22. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le Û \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. Set **(**$\beta_1, \beta_2, \ldots, \beta_n$**)** detects fault F if
A. $\exists j$, $1 \le j \le m$, $\ddot{} f^*(\beta_1, \beta_2, \ldots, \beta_n) \ne f_j(\beta_1, \beta_2, \ldots, \beta_n)$;
B. for $\forall(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *input patterns,* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, *and for* $\forall j$, $1 \le j \le m$, $f_Û^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \equiv f_j(\beta_1, \beta_2, \ldots, \beta_n)$;
C. for $\forall(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *input patterns, for* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, *and* $\forall j$, $1 \le j \le m$, $f_Û^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\beta_1, \beta_2, \ldots, \beta_n)$;
D. $\exists$ j, $1 \le j \le m$, *so that* $f_Û^*(\beta_1, \beta_2, \ldots, \beta_n) \le f_j(\beta_1, \beta_2, \ldots, \beta_n)$;

E. $\exists$ *j,* $1 \le j \le m$*, so that* $f_{\hat{U}}^*(\beta_1, \beta_2, \ldots, \beta_n) \ge f_j(\beta_1, \beta_2, \ldots, \beta_n)$.

7a23. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le \hat{U} \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. F fault cannot be detected with respect to some class faults if

A. $\exists$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such input pattern,* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\exists j$, $1 \le j \le m$*, and* $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

B. 1. F fault cannot be detected or

2. $\exists G \in \Phi$ *fault for which* $\exists$ *line B, for which in case of* $\forall (\alpha_1, \alpha_2, \ldots, \alpha_n)$ *input pattern,* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\forall j$, $1 \le j \le m$*, and* $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) = f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$*, where* $f_{\hat{U}}^{**}$ *is the function obtained from C when a fault G occurs on its line B*

C. 1. fault F is detectable;

2.for $\forall (\alpha_1, \alpha_2, \ldots, \alpha_n)$ *input patterns, for* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\forall j$, $1 \le j \le m$, $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

D. 1. fault F is detectable;

2. $\exists$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such input pattern,* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, ¨ $\exists j$, $1 \le j \le m$*, so that* $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \le f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

E. 1. fault F is detectable;

2. $\exists$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *such input pattern,* $\alpha_i \in \{0, 1\}, 1 \le i \le n$, ¨ $\exists j$, $1 \le j \le m$*, so that* $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ge f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

7a24. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le \hat{U} \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. F fault is not redundant if

A. for $\forall (\alpha_1, \alpha_2, \ldots, \alpha_n)$ *input patterns, for* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\forall j$, $1 \le j \le m$, $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

B. $\exists$ *input pattern* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ *so that* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\exists$ j, $1 \le j \le m$*, for which* $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

C. $\exists$*such input pattern* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\exists j$, $1 \le j \le m$*, that* $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) = f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

D. $\exists$ *such input pattern* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\exists j$, $1 \le j \le m$*, so that* $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \le f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

E. for $\forall$ *input pattern* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, $\exists j$, $1 \le j \le m$*, so that* $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ge f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

7a25. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le \hat{U} \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. Set T is not a test with respect to set Φ of faults if

A. $\exists f \in \Phi$ *so that for* $\forall (\alpha_1, \alpha_2, \ldots, \alpha_n)$ *input patterns, for* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\forall j$, $1 \le j \le m$, $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

B. for $\forall f \in \Phi$*, for* $\forall$ *input pattern* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$*, for* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\forall j$, $1 \le j \le m$, $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

C. for $\forall f \in \Phi$, $\exists$ *such input pattern* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\exists j$, $1 \le j \le m$*, so that* $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \le f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

D. for $\forall f \in \Phi$, $\exists$ *such input pattern* $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\exists j$, $1 \le j \le m$*, so that* $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ge f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

E. $\exists f \in \Phi$*, for which, and for* $\forall (\alpha_1, \alpha_2, \ldots, \alpha_n)$ *input pattern,* $\alpha_i \in \{0, 1\}, 1 \le i \le n$*, and* $\forall j$, $1 \le j \le m$, $f_{\hat{U}}^*(\alpha_1, \alpha_2, \ldots, \alpha_n) = f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

7a26. In combinational circuit which has N lines, any number of stuck-at-0 or stuck-at-1 faults can occur. Find all possible multiple (not single) number of faults.

A. 2^N

B. 3^N

C. 3^N - 1
D. 3^N - 2^N - 1
E. 2N

7a27. What is technical object model? B technical object is called A technical object model if through its experiments it is possible to have idea about A technical object's
A. design
B. properties
C. parameters
D. circuit
E. structure

7a28. In what sequence are the following stages of digital IC design executed? a) layout design, b) behavioral-level design, c) logic design, d) RTL design
A. c-a-b-d
B. d-b-c-a
C. b-d-c-a
D. c-a-d-b
E. a-b-c-d

7a29. In component level of IC design what kind of mathematical method is used?
A. probability theory
B. theory of queue system
C. Boolean algebra
D. differential equations system
E. partial differential equations system

7a30. In case of the given elemental bases, in what sequence does the consumption power increase if the other parameters are similar? a) bipolar; b) CMOS; c) N-MOS
A. b - c-a
B. a-c-b
C. a-b-c
D. b-a-c
E. c-b-a

7a31. Which of the given answers more contributes to the increase of performance in digital circuits?
A. decrease of load capacitance
B. increase of load capacitance
C. decrease of technological sizes
D. decrease of supply voltage
E. A. and C. together

7a32. Which of the given answers more characterizes the advantage of MOS elemental base in comparison to bipolar?
A. little consumption power
B. high performance
C. simplicity of technology
D. A and C together
E. A and B together

7a33. A password for a kindergarten net must contain 2 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 4 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?
A. 1 000 000
B. 2 000 000
C. 5 000 000
D. 8 000 000
E. 10 000 000

7a34. A password for a kindergarten net must contain 2 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 2 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?

A. 100 000
B. 400 000
C. 600 000
D. 800 000
E. 1 000 000

7a35. A password for a kindergarten net must contain 2 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 3 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?

A. 600 000
B. 800 000
C. 1 000 000
D. 1 200 000
E. 1 800 000

7a36. A password for a kindergarten net must contain 3 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 3 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?

A. 100 000
B. 1 000 000
C. 10 000 000
D. 100 000 000
E. 1 000 000 000

7a37. $\bar{x}_1\left(x_2\, x_3 \vee x_4\left(x_5 \oplus \bar{x}_6\right)\right)$ norm of function equals:

A. 3/32
B. 9/32
C. 5/36
D. 7/32
E. 11/32

7a38. $x_1 x_2\left(\bar{x}_3 \oplus x_4\left(\bar{x}_5 \vee x_6\right)\right)$ norm of function equals:

A. 3/16
B. 1/8
C. 5/8
D. 1/16
E. 3/4

7a39. $\left(x_1 \vee x_2\right) \oplus x_3\left(\bar{x}_4 \vee \bar{x}_5\right)\bar{x}_6$ norm of function equals:

A. 21/32
B. 25/32
C. 27/32
D. 11/32
E. 19/32

7a40. x_1 argument activity of $x_1\bar{x}_2\left(x_3 \vee x_4\bar{x}_5 x_6\right)$ function equals:

A. 5/32
B. 9/32
C. 9/16
D. 7/16
E. 19/32

7a41. x_3 argument activity of $x_1\bar{x}_2\left(x_3 \vee x_4\bar{x}_5 x_6\right)$ function equals:

A. 5/16
B. 11/32
C. 7/32

D. 5/32
E. 13/16

7a42. x_4 argument activity of $x_1\bar{x}_2\left(x_3 v x_4 \bar{x}_5 x_6\right)$ function equals:

A. 13/32
B. 1/32
C. 9/32
D. 7/32
E. 11/32

7a43. The activity of the combination of x_4 and x_5 arguments for $\left(\bar{x}_1 v x_2\right)\oplus\left(x_3 v x_4 \bar{x}_5\right)$ function equals:

A. 3/4
B. 1/4
C. 5/8
D. 5/16
E. 3/8

7a44. The activity of the combination of x_3 and x_4 arguments for $\left(\bar{x}_1 x_2\right)\oplus\left(x_3 v \bar{x}_4\right)x_5$ function equals:

A. 1/8
B. 7/8
C. 1/4
D. 3/4
E. 5/8

7a45. The activity of the combination of x_4 and x_5 arguments for $\left(\bar{x}_1 v \bar{x}_2\right)\oplus\left(x_3 v \bar{x}_4 \bar{x}_5\right)$ function equals:

A. 3/4
B. 1/4
C. 5/8
D. 1/8
E. 5/4

b) Problems

7b1.

Construct Zhegalkin polynomial for the threshold function with threshold w=3 and weights of variables ξ_1=2, ξ_2=2, ξ_3=2.

7b2.

Verify the completeness of $\{x_1 \vee x_2,\ x_1 \to x_2,\ x_1 x_2 \overline{x_3}\}$ function system.

7b3.

Using Post's theorem verify the completeness of $\{1,0,\bar{x},\ \left(x_1 \to x_2\right)\to x_3\}$ function system.

7b4.

Construct Zhegalkin polynomial of $\left(x_1 \to x_2\right)^{\bar{x}_3}$ function.

7b5.

Prove that for N bit number it is possible to calculate the number of 1-s for O(logN) time.

7b6.

Prove that in N bit number it is possible to calculate the number of 1s in O(M) time where M is the number of 1s.

7b7.
Prove that in unordered array K[th] search can be executed in linear time.

7b8.
Prove that ordering based on binary heap is executed in O(NlogN) time.

7b9.
Construct perfect disjunctive normal form of Boolean function given by 11011011 table.

7b10.
Construct Zhegalkin polynomial of the Boolean function given by 11011101 table.

7b11.
Cayley code of G tree by numbered nodes is given h(G)=(3,5,4,4,5,6,7,8). Reconstruct the tree.

7b12.
Check the completeness of $\{ x_1^{x_2} \vee x_2^{x_3}, x_1\bar{x}_2, x_1 \mapsto x_2 \}$ function system.

7b13.
Cayley code of G tree by numbered nodes is given h(G)=(3,2,4,4,5,6,8,8). Reconstruct the tree.

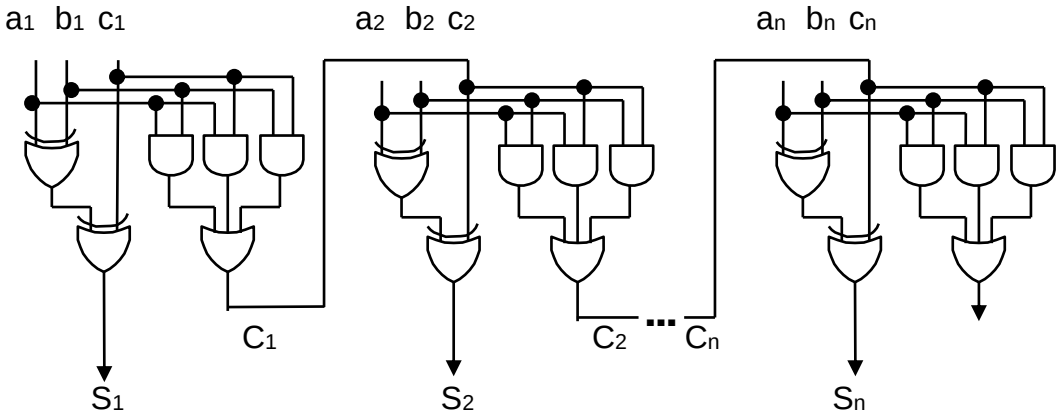
7b14.
Check the completeness of $\{ x_1^{x_3} \vee x_2^{x_1}, x_1 \to \bar{x}_2, x_1 \oplus x_2 \}$ function system.

7b15.
Calculate arguments' $\xi_1 = 2, \xi_2 = 5, \xi_3 = 7, \xi_4 = 10$ balances and argument activities having w=10 threshold function.

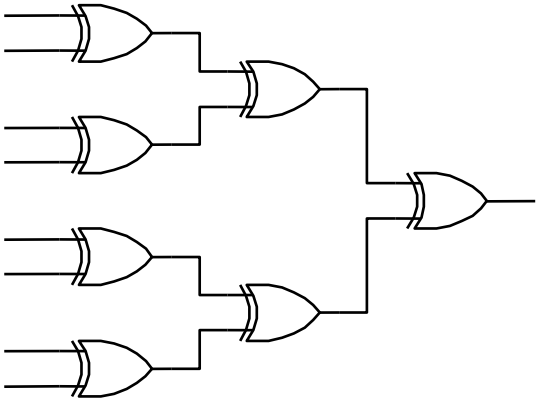
7b16.
Check the completeness of $\{ x_1 x_2, x_1 \to x_2, x_1 \oplus x_2, x_1 \vee x_2 \}$ function system.

7b17.
Given an n-input Boolean function $f(x_1, x_2, \ldots, x_n) = x_1 \oplus x_2 \oplus \ldots \oplus x_n$. Construct the Binary Decision Diagram for $f(x_1, \ldots, x_i, \ldots, x_n)$.

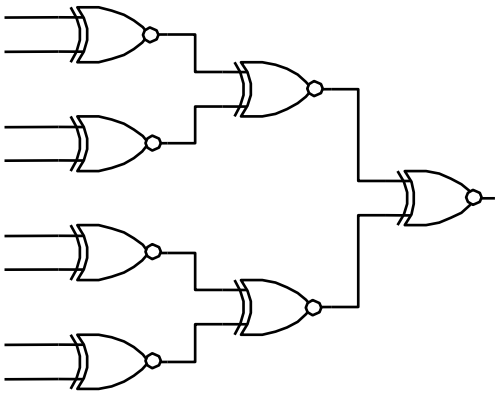
7b18.
Figure depicts the circuit of an n-bit adder. Prove that all possible single stuck-at-0 and stuck-at-1 faults on all lines of that circuit can be detected by means of only 8 test vectors.



7b19.
Figure depicts the circuit of an N-input parity tree. Prove that all possible single stuck-at-0 and stuck-at-1 faults on all lines in that circuit can be detected by means of only 4 test vectors.

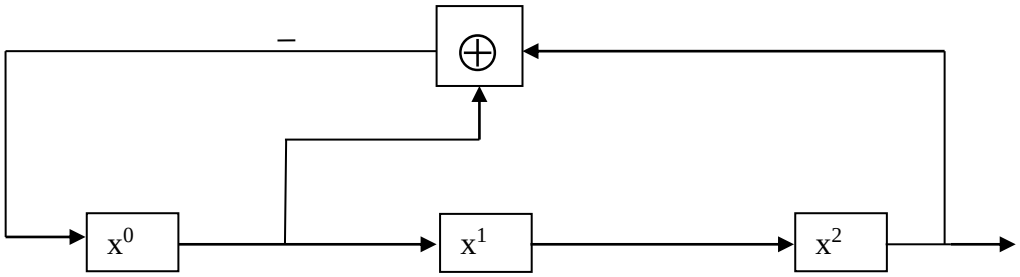


7b20.
Figure depicts the circuit of N-input tree with negated Modulo 2 elements (gates XOR). Prove that all possible single stuck-at-0 and stuck-at-1 faults on all lines of that circuit can be detected by means of only 4 test vectors.

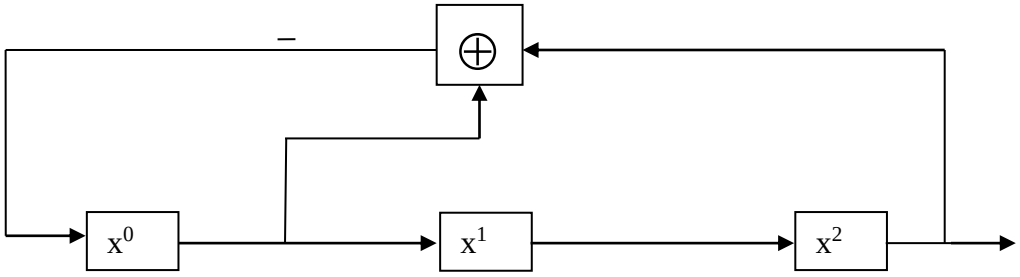


7b21.
The given combinational circuit has 1000000 lines. Constant 0 or constant 1 faults of random numbers can occur there. Find the number of all possible multiple faults.

7b22.
Given a Linear Feedback Shift Register corresponding to characteristic polynomial $1+x+x^3$. Find the subsets of all patterns which are generated by the given LFSR.



7b23.
Given a Linear Feedback Shift Register corresponding to characteristic polynomial $1+x+x^3$. Transform yhr circuit, adding elementary cell(s) in a way that the obtained new circuit generates one set, consisting of all patterns.



7b24.
Construct Zhegalkin polynomial of the Boolean function given by $f = x_1 \oplus x_3^{x_1 \vee x_2}$.

7b25.
By root tree's 000101001111 code, reconstruct that tree.

7b26.
Calculate arguments activities of $x_1 x_2 \oplus (x_1 \vee x_2 x_3)$ function.

7b27.
Cayley code of G tree by numbered nodes is given h(G)=(2, 3, 3, 4, 5, 5, 8)
Reconstruct the tree.

8. OBJECT-ORIENTED PROGRAMMING

a) Test questions

8a1. You are charged with writing a function that needs to be able to write to both standard output (typically the console screen) and files. Referring to the scenario, which one of the following function declarations satisfies that need?

A. void print(cout);
B. void print(ostream &os);
C. void print(istream &is);
D. void print(ofstream ofs);
E. void print(istream is);

8a2. After performing the below mentioned code, which is the value of n?
int n = !(!5 & !7)

A. false
B. 1
C. 3
D. 5
E. It contains an error. After using ! operator, constant values should be definitely taken in brackets, e.g.(!5)

8a3. Small function is present, which is often called from several special places. How can the implementation of the codes be accelerated which use the given function?

A. Make function virtual
B. Replace floating point computation of integer numbers, to use FPU device
C. Reduce the use of automat variables
D. Make all the variables of that function volatile
E. Make function inline

8a4. Which is the difference between non-specialized function's member and constructor?

A. Constructor can return values, and member-functions - no
B. Member-functions can define values, constructors – no.
C. Constructor can define values, and member-functions - no
D. Member-functions can return values, and constructors - no
E. Constructor can announce values, and member-functions - no

8a5. const int x= 0xFFFE;
int y = 2;
int z = x&&y;
Which is the value of z, in terms of the above code?

A. 0
B. 1
C. 2
D. 3
E. 4

8a6. Which of the below mentioned statements concerning overloading of ++ operator is true?

A. It is impossible to overload prefix ++ operator
B. It is impossible to overload postfix ++ operator
C. It is necessary to use additional int type parameter to overload ++ postfix operator
D. It is always necessary to create prefix ++ operator
E. It is impossible to overload both prefix and postfix ++ operators for one class.

8a7. Binary search complexity is

A. O(logN), where N is the number of elements
B. O(NlogN)
C. O(N)
D. $O(N^2)$
E. The correct answer is missing

8a8. The complexity of Prim's algorithm is

A. O(|E|)
B. $(|V|^2)$

C. O(|E||V|)*
D. O(|E|+|V|)
E. The correct answer is missing

8a9. When the class is inherited from base as public, which of the below mentioned statements is right?
A. All the members of base class become public members of inherited class
B. All the members of inherited class become public members of base class
C. All the protected members of base class are protected members of inherited class
D. All the members of base class become protected members of inherited class
E. All the members of inherited class become private members of base class

8a10. The ability to invoke a method of an object without knowing exactly what type of object is being acted upon is known as which one of the following?
A. Encapsulation
B. Class relationship
C. Inheritance
D. Polymorphism
E. Friend relationship

8a11.
```
class X
{
  int I;
public:
  int f() const;
};
int X::f() const {return I++;}
```
Where is an error in the above written code?
A. X::f member-function must be static
B. X::f member-function is constant but changes non-mutable data-member of the object
C. X::I data-member lacks access specifier
D. X::f member-function cannot change as it lacks access specifier
E It is not possible to change the integer I as it lacks access specifier

8a12. The complexity of quick sorting algorithm for the worst case will be
A. O(logN), where N is the number of elements
B. O(NlogN)
C. O(N)
D. $O(N^2)$
E. The correct answer is missing

8a13.
```
class Base {
public:
  Base();
  ~Base();
  int getBaseNum();
private:
  int baseNum;
};

class A : public Base{
public:
  A();
  ~A()
  float getBaseNum();
private:
  float baseNum;
};
```
Which concept is presented through the code in the example?
A. Recursion
B. Polymorphism
C. Inheritance
D. Reloading of functions

E. Virtual functions

8a14. int i = 4, x = 0;
do {
  x++;
} while(i--);
What is the value of X after performing the above written code?
A. 5
B. 4
C. 0
D. Infinite
E. There is syntax error while cycle cannot be formed as mentioned above

8a15. The complexity of Floyd algorithm is
A. $O(N^3)$, where N is the number of nodes
B. O(NlogN)
C. O(N)
D. $O(N^2)$
E. The correct answer is missing

8a16. The complexity of subline search in Knut-Morris-Pratt algorithm on average will be (n – length of the line, m – length of the subline)
A. O(n)
B. O(m)
C. O(n+m)
*D. O(n*m)*
E. The correct answer is missing

8a17.
```
class MyClass
{
public:
  MyClass();
  virtual void MyFunction()=0;
};
```
Which is the below written statements is correct for the given code?
A. MyClass is a pure virtual class
B. Class definition is wrong
C. MyClass is a virtual base class
D. Function returns value
E. MyClass is an abstract class

8a18. Which of the below written statements is correct for function overloading?
A. Although the return type can be modified, the types of the parameters can as well. The actual number of parameters cannot change.
B. Function overloading is possible in both C++ and C
C. Templates and namespaces should be used to replace occurrences of function overloading.
D. Overloaded functions may not be declared as "inline."
E. The compiler uses only the parameter list to distinguish functions of the same name declared in the same scope.

8a19. The complexity of Dexter algorithm is
A. $O(|E|)$
B. $O(|E|*|V|)$
C. $O(|V|^2)$
D. $O(|E|+|V|)$
E. The correct answer is missing

8a20. Assume an algorithm determines the number of triangles formed by *n* points in the plane. What is the maximal possible output of A for n=7?
A. 35
B. 27
C. 17
D. 15

E. The correct answer is missing

8a21. What is the difference between class and struct?
A. Class must contain constructor, and struct may not have it
B. Struct does not have inheritance opportunity
C. Struct does not have deconstructor
D. By default input specificators are distinguished
E. No difference

8a22. Which is the value of z in case of the code below?
```
const int x= 012;
int z = 1 << x;
```
A. 0
B. 1024
C. 4096
D. 2048
E. It contains an error and will get compilation error

8a23. Which of the mentioned cycles is infinite?
A. for (int i=1;i>23;i++);
B. for (int i=0;i>=1;i++);
C. for (int i=10;i>6;i++);
D. for (int i=5;i>15;i++);
E. All the cycles are finite

8a24. After performing the code below, what will be displayed on the screen? (assume sizeof(int) = 4)
```
#include <iostream>
using namespace std;

void main()
{

   int (*p)[10]= {NULL};
   int k= int((size_t)(p+1) - (size_t)p);

         cout<<k<<endl;

}
```
A. 1
B. 2
C. 4
D. 10
E. 40

8a25. Which of the mentioned ones is not heredity access attribute
A. public
B. private
C. virtual
D. protected
E. All are heredity access attribute

8a26. For a given pair of integers *n, k* it is calculated n^k. Assuming that calculation uses only multiplications, show the minimal number of multiplications among represented in the table that is enough to calculate 5^{1024}.
A. 12
B. 11
C. 10
D. 9
E. 8

8a27. After performing the code below, which is the value of n?
```
Int i = 5;
int n = i++-1;
```

A. 6
B. 5
C. 4
D. 3
E. It contains an error and will get compilation error

8a28. After performing the code below, which is the value of b?

```
#include <iostream>
using namespace std;

void main ()
{
        int a = 0;
        int b = 2;

        switch (b)
        {
                case 1:
                        a=1;
                        break;
                case 2:
                        int b=0;
        }
}
```

A. 0
B. 1
C. 2
D. There is syntax error, switch is not possible to form as described above
E. The program will work infinitely

8a29. Which of the mentioned is not C++ data type?
A. unsigned long
B. unsigned short
C. unsigned char
D. unsigned int
E. All are C++ data types

8a30. Which of the mentioned is not one of the basic clauses of object-oriented programming?
A. Encapsulation
B. Typification
C. Inheritance
D. Polymorphism
E. All the mentioned belong to the basic clauses of object-oriented programming.

8a31. An algorithm is developed that for any given list of natural numbers L = {a_1, …, a_n} finds the maximum, minimum elements and the arithmetical average value of L. What is the minimal number of passes in reading L that is enough get the output in the algorithm?
A. 5
B. 4
C. 3
D. 2
E. 1

8a32. After performing the code below, which is the value of n?

```
int n = 1 << 3 * 2 + 1;
```

A. 1
B. 17
C. 65
D. 128
E. It contains and error and will get compilation error

8a33. To classify the following 1,2,3,5,4 sequence ascending, it is more appropriate to use
A. Quick Sort
B. Bubble Sort

C. Merge Sort
D. Heap Sort
E. No appropriate version

8a34. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
using namespace std;
double A;
void main ()
{
        int A;
        A=5;
        ::A = 2.5;
        cout<<A<<"   "<<::A;
}
```

A. 5 2.5
B. 2.5 5
C. 5 5
D. 2.5 2.5
E. The program contains syntax error

8a35. How much is the complexity of algorithm to add element in binary tree?
A. $O(N^2)$, where N is the number of nodes
B. O(logN)
C. O(N)
D. O(1)
E. The correct answer is missing

8a36. An algorithm is developed that for any given list of natural numbers L = {a_1, …, a_n} finds the sum $\sum_{i=1}^{n}(a_i - \overline{a})^2$, where $\overline{a}$ denotes the arithmetical average of the elements list L: What is the floor amount of passes enough to calculate the output?
A. 1
B. 2
C. 3
D. 4
E. 5

8a37. Which of the statements is correct?
A. Class cannot have 2 constructors
B. Class cannot have 2 destructors
C. Virtual destructor does not exist
D. All the above mentioned statements are correct
E. All the above mentioned statements are wrong

8a38. The complexity of Merge Sort algorithm in the worst case will be:
A. O(NLogN)
B. $O(N^2)$
C. O(N)
D. $O(N^3)$
E. The correct answer is missing

8a39. After performing the code below, what will be displayed on the screen?

```
#include <stdio.h>
class a
{
public: virtual void print() {printf("a");}
};
class b: public a
{
public: virtual void print() {printf("b");}
```

```
};

int main()
{
   b b0;
   a a0= b0, &a1= b0;
   a0.print();
   a1.print();
   return 0;
}
```

A. aa
B. ab
C. bb
D. ba
E. The program contains syntax error

8a40. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
using namespace std;

void main()
{

   int c = 1;
   c= ++c + ++c;
         cout<<c;
}
```

A. 2
B. 3
C. 4
D. 5
E. 6

8a41. What is the output of the following part of the program?

```
cout << (2 | 4 ^ ~3 );
```

A. 0
B. 1
C. 2
D. 3
E. the correct answer is missing

8a42. How many errors are below?

```
class B {}
class A
         :  public B
{
         int m_value
         int get_value(int = 0)
         {
                  return m_value;
         }
}
int main () {
         A a();
         a = a;
         a.*get_value();
         return 0;
}
```

A. 3
B.4
C. 5
D. 6

E. 7

8a43. What is (7 >> 1 << 1) expression value?
A. 5
B. 6
C. 7
D. 8
E. the correct answer is missing

8a44. What is the output of the following part of the program?

```
int n = 5;
switch(n)
{
        case '5':
                cout << "A \n";
                break;
        case 5:
                cout << "B \n";
        default:
                cout << "C \n";
                break;
}
```

A. A
B. B
C. C
D. BC
E. AC

8a45. Complexity of “merge” sorting algorithm
A. linear
B. constant
C. logn
*D. n*logn*
E. square

8a46. int n = !(!5 & !7)
What is the value of n after performing the code above?
A. false
B. true
C. 0
D. 1
E. It has an error. Using ! operator, constant values must be written in brackets. For example, (!5)

8a47. Complexity of adding element in search balanced binary tree
A. linear
B. constant
C. logn
*D. n*logn*
E. square

8a48.

```
int i = 4, x = 0;
do{
  x++;
}while(i--);
```

after executing the above written code, which is the value of X?
A. 0
B. 1
C. 3
D. 4
E. 5

8a49. class MyClass

```
{
public:
 MyClass();
 virtual void MyFunction()=0;
};
```

Which statement is true for the above mentioned code?

A.Class definition is wrong
B. MyClass is a virtual class
C. MyClass is a virtual base class
D. MyClass is an abstract class
E. the correct answer is missing

8a50. What is the value of (13 >> 1 << 1) expression?

A. 11
B. 12
C. 13
D. 14
E. 15

8a51. How many errors does the following part contain?

```
class A
        :  int
{
        int m_value
        int get_value(int = 0)
{
        return m_value;
}
}
int main () {
        A a();
        a = a;
        a->get_value();
return 0;
}
```

A. 2
B. 3
C. 4
D. 5
E. 6

b) Problems

8b1.

Develop a program that, given two symbol sequences, finds the length of the longest common subsequence of the given sequences
For example,
SYNOPSYS, SINOPSYS → 7

8b2.

Assume A is the known W. Ackermann function:

$$A(0, y) = y + 1;$$

$$A(x, 0) = A(x - 1, 1);$$

$$A(x + 1, y + 1) = A(x, A(x + 1, y)).$$

Redefine A in a way that it is computed modulo 7717.

$$AM(x, y) = A(x, y) \ \ Mod(7717),$$

Restrict the enormous growth of A.
Develop a program that can compute AM(10,10) in several seconds and find the value of AM(10,10).

8b3.
Assume Fib is the Fibonacci function:

$$Fib(n) = \begin{cases} 1, & if \quad n = 1 \text{ or } n = 2; \\ Fib(n-1) + Fib(n-2), & otherwise. \end{cases}$$

Define the number Q as follows:

$$Q = \sum_{k=1}^{11} (1 / Fib(Fib(k))).$$

Calculate the number Q with an accuracy guaranteeing that the sum of the first 36 decimal digits can be computed exactly.

8b4.
Develop an algorithm that for any given pair of natural numbers n ≥ k constructs the set of all the subsets of {1,2,…,n} having cardinality equal to k.

8b5.
Prove (using induction argument) that the following algorithm for exponentiation is correct.
function power (y,s)
comment Return y^z, where $y \in R$, $z \in N$
x:=1;
while z > 0 do
if z is odd then x := x * y;
z:= ⌊z/2⌋;
$y:=y^2$;
return(x)

8b6.
Prove (using induction argument) that the following algorithm for the multiplication of natural numbers is correct.
function multiply (y, z)
comment Return y*z, where $y,z \in N$
x:=0:
while z > 0 do
*x := x + y * (z* mod 2);
y:=2y; z:= ⌊z/2⌋;
return(x)

8b7.
Prove (using induction argument) that the following algorithm for the multiplication of natural numbers is correct.
function multiply(y, z)
comment Return the product y*z.
If z = 0 **then return**(0) else
return(multiply(2y, ⌊z/2⌋ + y*(z mod 2))

8b8.
Write a program which, given a sequence of integers, finds the length of the longest increasing subsequence.
Input
Input contains length of sequence 0<N<1000, then follows N integers, does not exceed 109 by absolute.
Output
Write one number in the output, length of the longest increasing subsequence.
Example

Input	Output
5	3

7 1 5 2 3

8b9.
Assume F is a Fibonacci sequence.
F0 = 1;
F1 = 1;
FN = FN-1 + FN-2 N>1
Write a program to find N-th Fibonacci number modulo 1000007. 0 < N < 109
Example
N = 5 F5 % 1000007 = 8

8b10.
Given a positive integer N.
Write a program to count the number of positive integers, not exceeding N and not divisible none of the given integers: 2,3,5.
Input
Input contains one integer N (1≤N≤2000000000).
Output
Output one number, answer for the given N.
Example

Input	Output
10	2

8b11.
Develop a detailed flowchart for an algorithm computing the greatest common divisor for a pair of positive integers, avoiding deletion operation.

8b12.
Assume a digital image is given by means of M = $||m_{ij}||$ n×n matrix where m_{ij} are non-negative integers.

a. Develop a detailed flowchart for an algorithm that finds the (rounded) coordinates of the centre of gravity of the image. Define needed auxiliary functions.

b. Evaluate the complexity of the developed algorithm.

8b13.
Assume for any integer $m \geq 2$ *P(m)* is a result of attaching consequtive positive integers represented in *m*-ary form. For example, the beginning part of *P(3)* looks as follows:

$$\underbrace{1}_{1}\ \underbrace{2}_{2}\ \underbrace{10}_{3}\ \underbrace{11}_{4}\ \underbrace{12}_{5}\ \underbrace{20}_{6}\ \underbrace{21}_{7}\ \underbrace{22}_{8}\ \underbrace{100}_{9}\ \underbrace{101}_{10}\ \underbrace{110}_{11}\ \mathrm{L}$$

Develop a detailed flowchart for an algorithm that given $m \geq 2$ and $n \geq 1$ finds the numeral allocated at n-th place in *P(m)* . Define needed auxiliary functions.

8b14.
A sequence is said to be a *polyndrome* if it has the central symmetry. Develop a detailed flowchart for an algorithm that given binary sequence *S* finds a longest segment of *S* that is a palindrome. If there are several such segments then it is enough to find one of them and the length of it.

8b15.
Print out all simple numbers not exceeding 1000. Natural number is called simple if it has exactly two dividers.

8b16.
Print out all perfect numbers not exceeding 1000. Natural number is called perfect if it equals the sum of all its dividers. For example, 6 = 1 + 2 + 3.

8b17.
Check if the given n number is symmetric or not (n < 107). The number is symmetric if it is read the same way from the beginning and the end. For example, 7586857.

ANSWERS TO TEST QUESTIONS
AND
SOLUTIONS OF PROBLEMS

1. DIGITAL INTEGRATED CIRCUITS

a) Test questions

1a1. B
1a2. D
1a3. E
1a4. B
1a5. A
1a6. C
1a7. B
1a8. B
1a9. D
1a10. A
1a11. A
1a12. D
1a13. C
1a14. B
1a15. E
1a16. A
1a17. C
1a18. E
1a19. A
1a20. C
1a21. D
1a22. B
1a23. D
1a24. E
1a25. E
1a26. B
1a27. B
1a28. D
1a29. B
1a30. C
1a31. B
1a32. E
1a33. D
1a34. D
1a35. C
1a36. D
1a37. C
1a38. C
1a39. A
1a40. D
1a41. A
1a42. D
1a43. D
1a44 B
1a45 E
1a46 E
1a47 B
1a48. C
1a49. B
1a50. E
1a51. A
1a52. C
1a53. C
1a54. E
1a55. B
1a56. B
1a57. D
1a58. C
1a59. C
1a60. C
1a61. B
1a62. D
1a63. C
1a64. D
1a65. C
1a66. B
1a67. B
1a68. B
1a69. C
1a70. D
1a71. A
1a72. B
1a73. D
1a74. B
1a75. A
1a76. A
1a77. E
1a78. B
1a79. C
1a80. B
1a81. C
1a82 B
1a83. B

b) Problems

1b1.

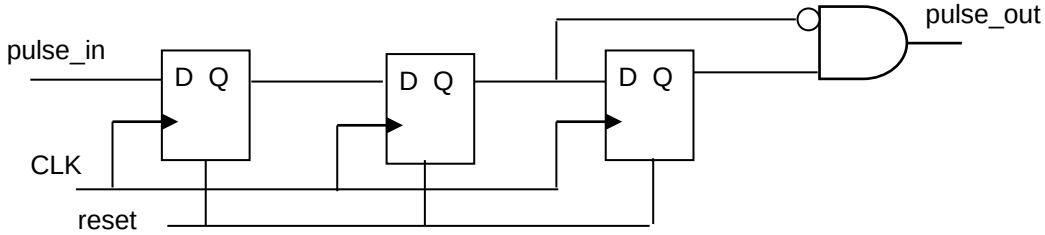
$t_{suX}=t_{bf}+t_{nor}+t_{su}-t_{clkbf}=2+7+4-3=11$ ns

$t_{hdX}=t_{clkbf}+t_{hd}-t_{bf}-t_{nor}=3+5-2-7=-1$ ns

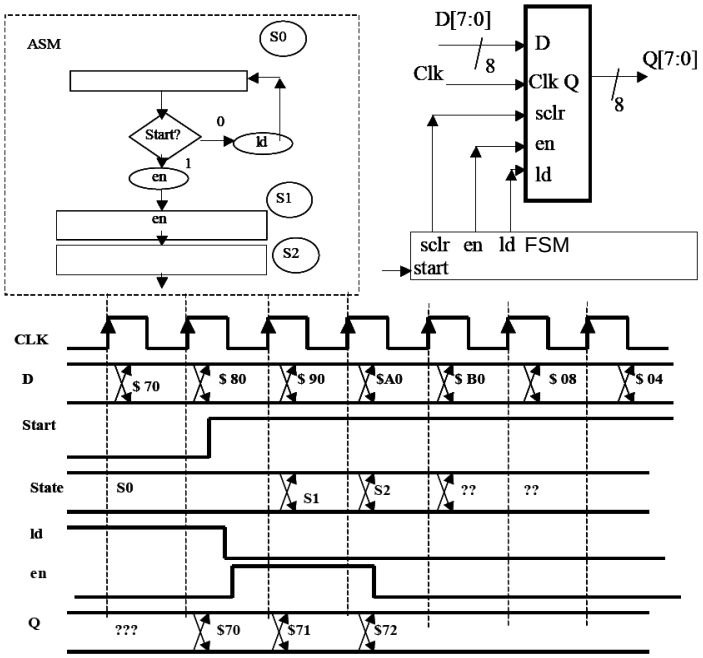
$t_L=t_{clkbf}+t_{CQ}+t_{or}=3+6+8=17$ ns

$t_{cycle}=t_{CQ}+t_{nor}+t_{su}=6+7+4=17$ ns

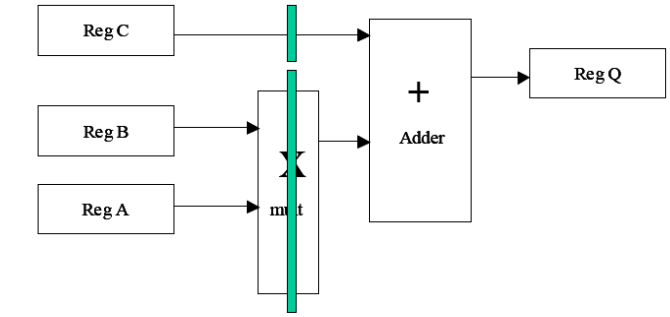
1b2.

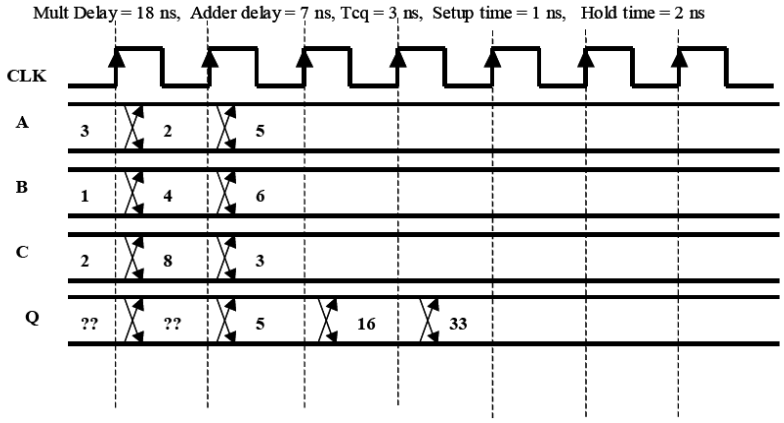


1b3.

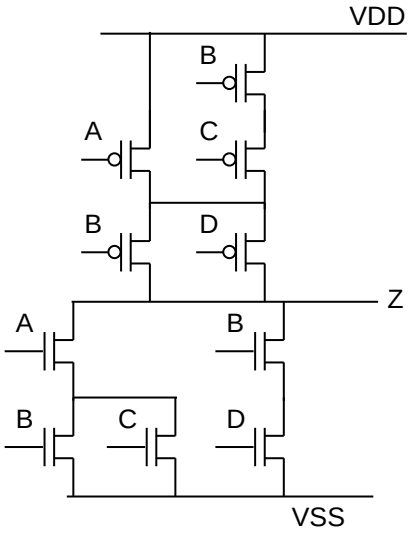


1b4.



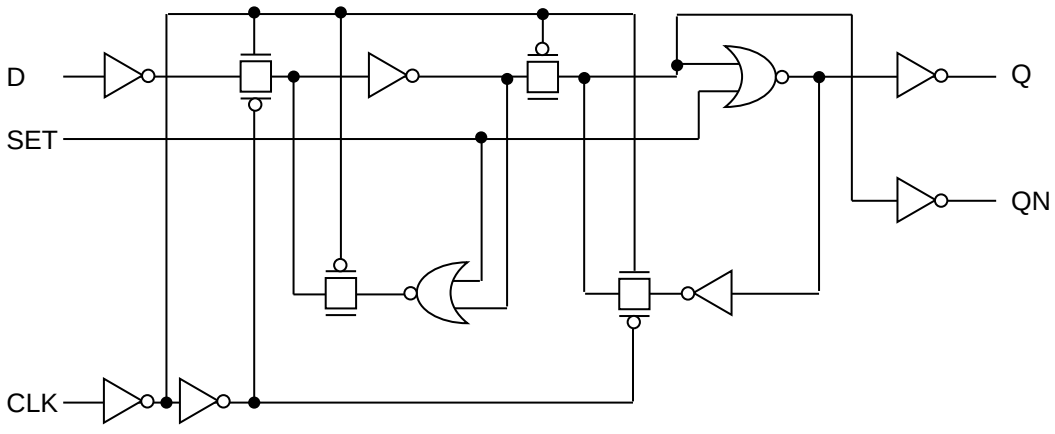


1b5.

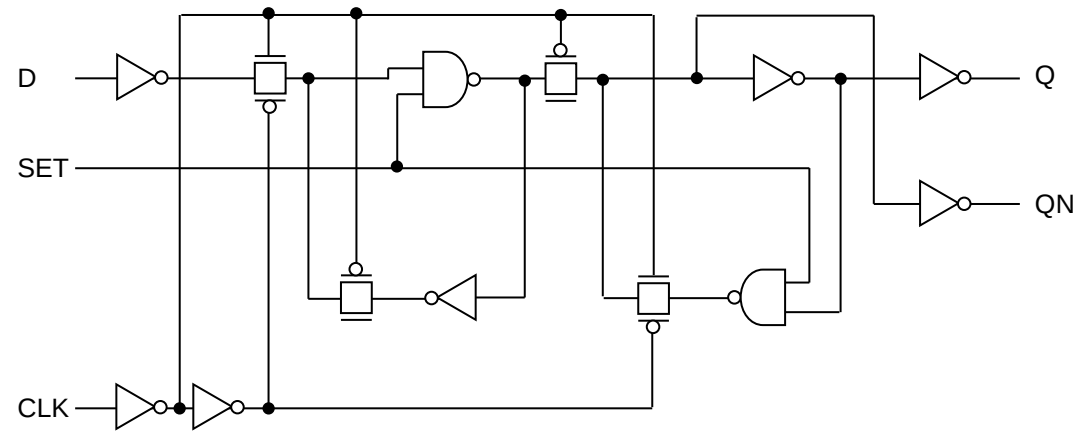


1b6.

D Flip Flop with High Active Set, v.1

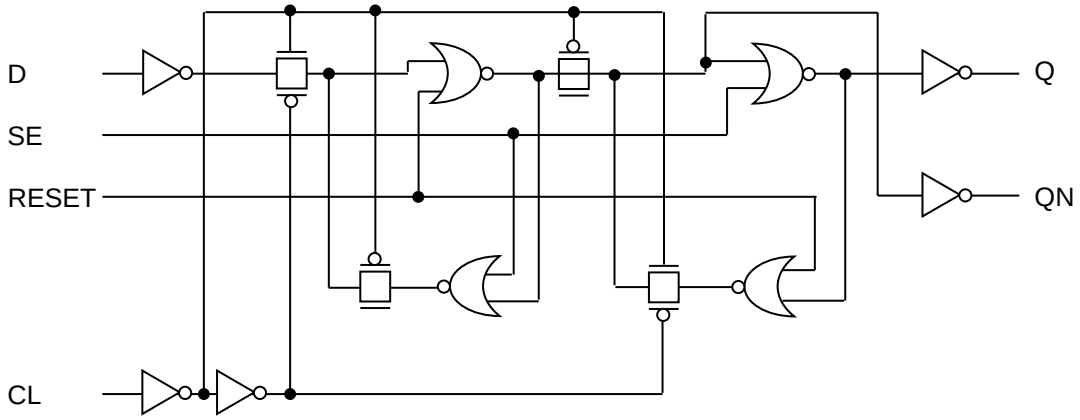


D Flip Flop with High Active Set, v.2

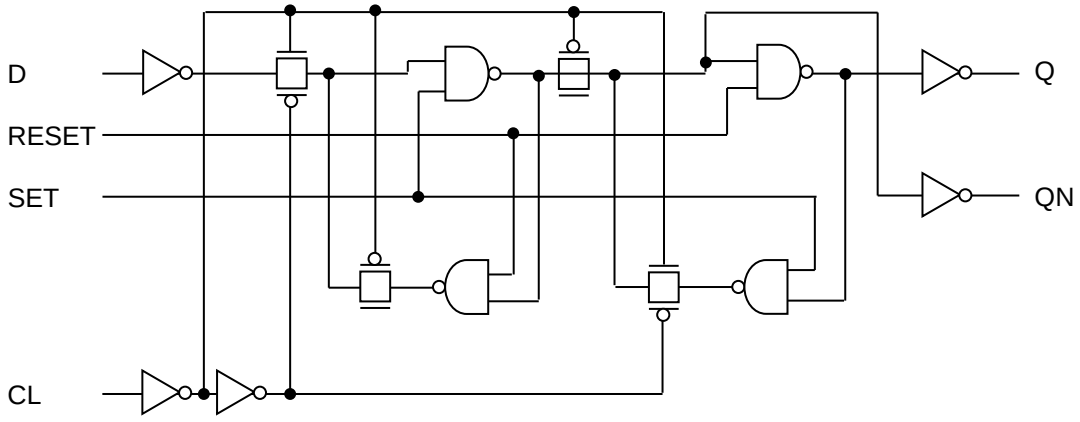


1b7.

D Flip Flop with High Active Set and Reset, v.1



D Flip Flop with High Active Set and Reset, v.2

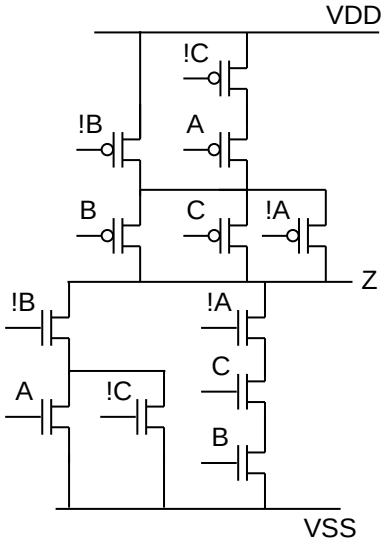


1b8.

A	B	C	Z	!Z
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0

0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Z=A&B+!C&B+!A&!B&C=!(!B(A+!C)+!A&B&C)



1b9.

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}},\ \beta = kp\frac{W}{L}$$

$$V_{SP} = \frac{\sqrt{\frac{kpn}{kpp}\frac{\frac{W_n}{L_n}}{\frac{W_p}{L_p}}} \cdot V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{kpn}{kpp}\frac{\frac{W_n}{L_n}}{\frac{W_p}{L_p}}}} = \frac{\sqrt{\frac{kpn}{kpp}} \cdot \sqrt{\frac{W_n}{W_p}} \cdot V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{kpn}{kpp}} \cdot \sqrt{\frac{W_n}{W_p}}} =$$

$$= \frac{\sqrt{\frac{kpn}{kpp}} \cdot \sqrt{\frac{W_n}{W_p}} \cdot 0.6 + (5 - 0.8)}{1 + \sqrt{\frac{kpn}{kpp}} \cdot \sqrt{\frac{W_n}{W_p}}} \approx \frac{\sqrt{\frac{1}{3}} \cdot 0.6 \cdot \sqrt{\frac{W_n}{W_p}} + 4.8}{1 + \sqrt{\frac{1}{3}} \cdot \sqrt{\frac{W_n}{W_p}}} \approx \frac{4.8}{1 + \sqrt{\frac{1}{3}} \cdot \sqrt{\frac{W_n}{W_p}}}$$

1. W_n=3 um

$$V_{SP3} = \frac{4.8}{1 + \sqrt{\frac{1}{3}} \cdot \sqrt{\frac{3}{10}}} = 3.64\ \text{V}$$

2. W_n=12 um

$$V_{SP12} = \frac{4.8}{1+\sqrt{\frac{1}{3}}\cdot\sqrt{\frac{12}{10}}} = 3.93\text{V}$$

$V_{SP12} < V_{SP3}$

$$\frac{W_p}{W_n} = \frac{10}{12} \qquad \frac{W_p}{W_n} = \frac{10}{3}$$

Therefore, the inverter corresponds to the left curve for which W_n=12 um.

1b10.

For both circuits the best case delay is the delay from input C to output Y.
For the shown NAND cell the delay from A input to Y output is smaller than from B input. Therefore, the best case delay of the 2nd circuit is smaller.

1b11.

The frequency of the ring oscillator is defined by the following formula:

$$f = \frac{1}{(t_{PHL1} + t_{PLH1}) + (t_{PHL2} + t_{PLH2}) + ... + (t_{PHLn} + t_{PLHn})},$$

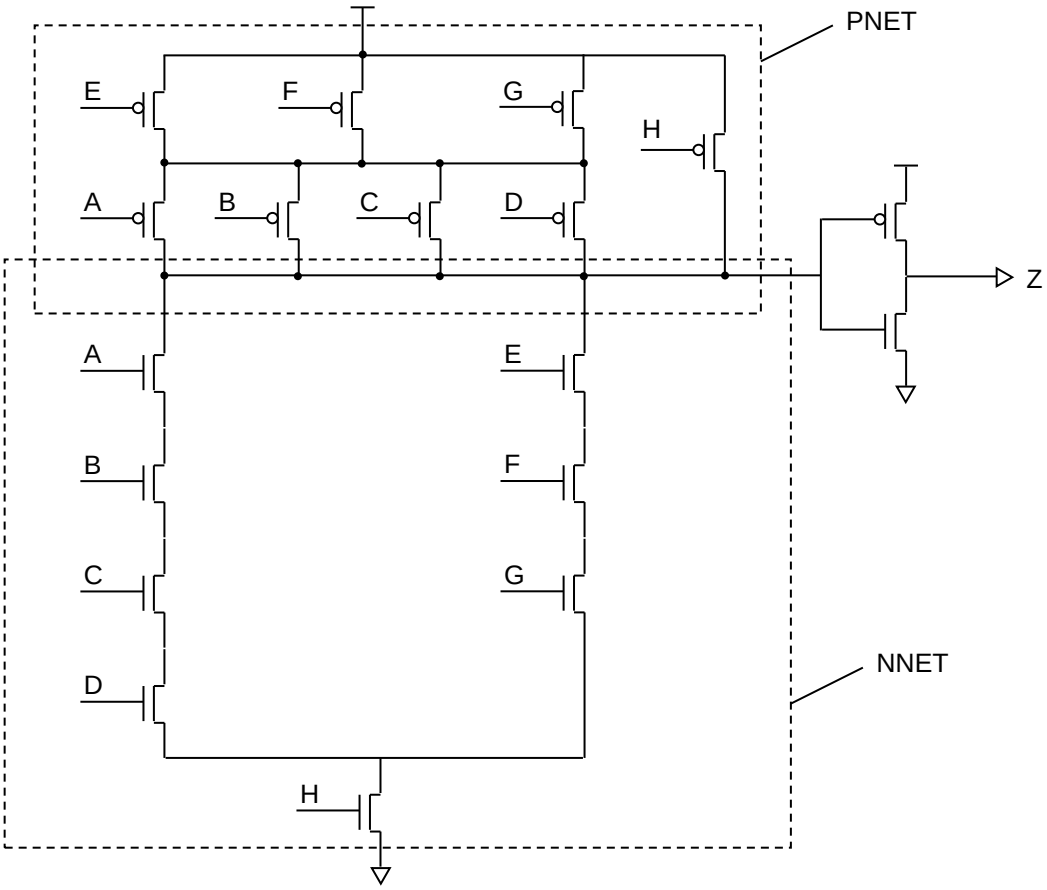
where t_{PHLi} and t_{PLHi} are the delays of i-th inverter's output and fall accordingly.
The number of inverters in a ring oscillator must be odd, so the 1st and 2nd circuits are not included in the ring oscillator (in operation, logic "1" is given to set input and the output NAND cell operates as an inverter).
The delay from a input to the output of the used NAND cell is smaller than the delay from b input to the output, so the 4th ring oscillator is the fastest.

1b12.

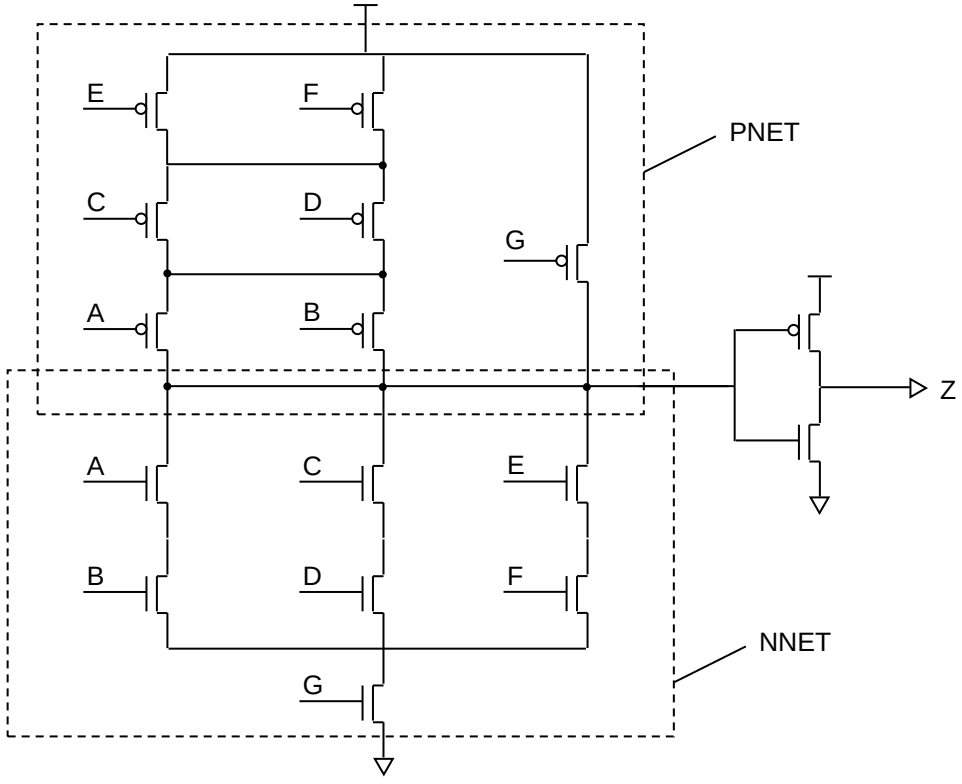
a. In order to get the signal from I12 in Q and QN, it is necessary to have the correct logic state in I22 and I23 feedback until CK fall transition. To say it otherwise, it is necessary to keep CK constant until the signal "passes" I3-I17-I23-I22 path. What us more, the signal level in I22 and I23 cells' outputs must be either 0.9 VDD or 0.1 VDD (VDD is supply voltage).
   Thus, CK mustn't switch at
   $\max(t_{PHL}I3+t_{PLH}I17,\ t_{PLH}I3+t_{PHL}I17)+\max(t_{rise}I23+t_{fall}I22,\ t_{fall}I23+t_{rise}I22)$=1650 ps.

b. As explained in item a., in this case also D must remain constant at
   $\max(t_{PHL}I1+t_{PLH}I11,\ t_{PLH}I1+t_{PHL}I11)+\max(t_{rise}I13+t_{fall}I12,\ t_{fall}I13+t_{rise}I12)-$
   $-t_{PLH}I12$=1250 ps.

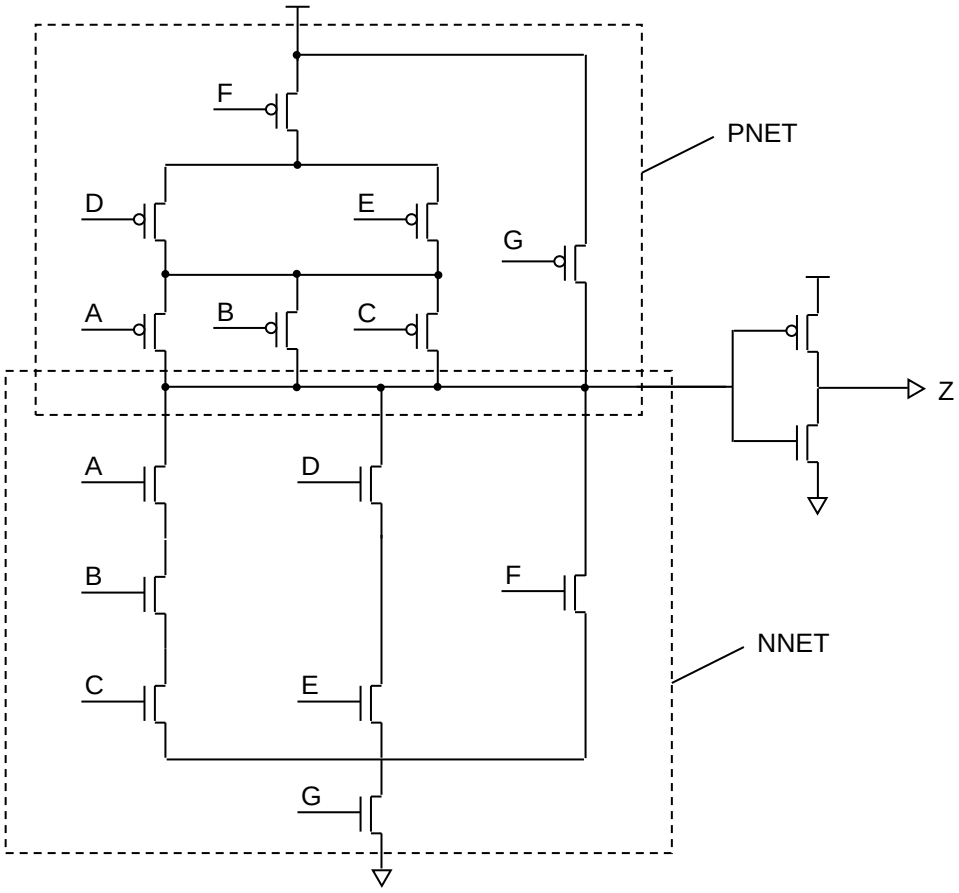
1b13.



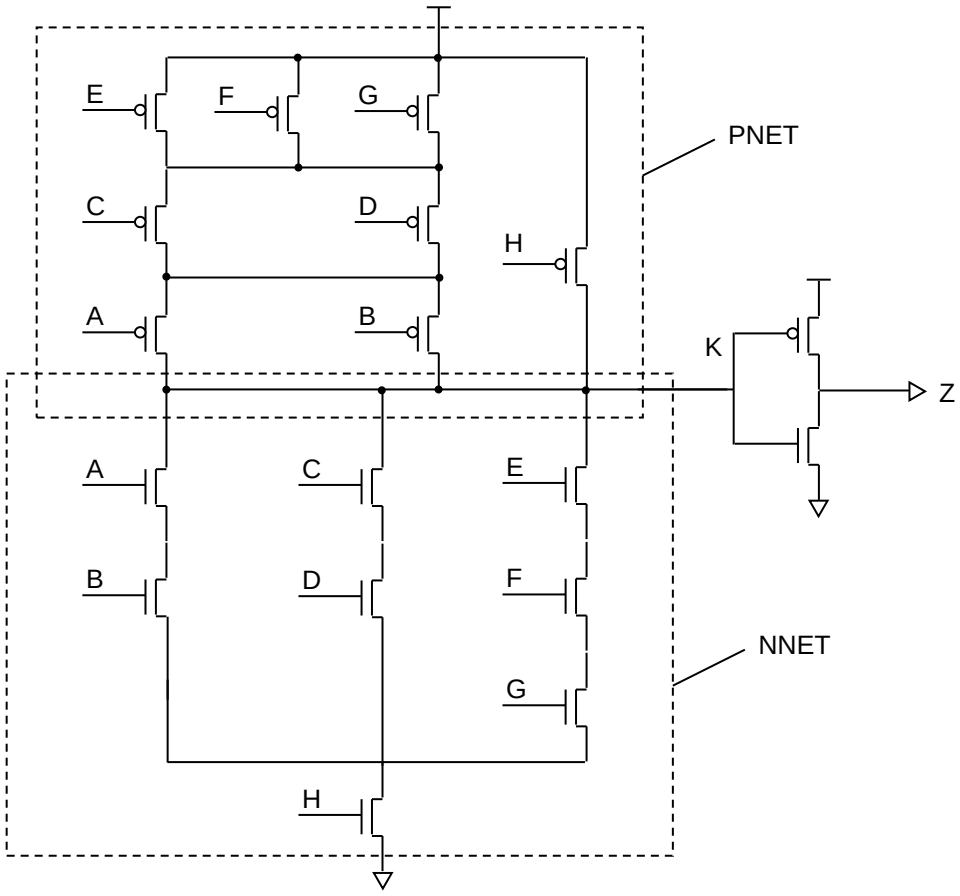
1b14.



1b15.



1b16.



P and N parts of the given circuit do not have common Euler path. For P net, Euler path is the following: H, E, F, G, C, A, B, D. For N net - H, B, A, C, D, E, F, G.

1b17.

The total charge of C_s and C_{BL} before M1 is on.

$$Q = C_s V_s + C_{BL} VDD/2$$

After M1 is on the voltages across C_s and C_{BL} are equalized to V_{BL}.

$$V_{BL}(C_S+C_{BL})=C_S V_S+C_{BL} VDD/2$$

When reading "1", $V_s=V_{DD}-V_t=1.2-0.3=0.9V$

$$V_{BL} = \frac{C_s V_s + C_{BL} VDD/2}{C_s + C_{BL}} = (0.9Cs+0.6*10Cs)/)Cs+10Cs)=6.9/11=0.63V$$

When reading "0", $V_s=0$

$$V_{BL}=0.6*10Cs/11Cs=0.55V$$

1b18.

$R=2V_{DD}\cdot L/W\cdot k\,(V_{DD}-V_t)^2$; $R_1=2\cdot 2.5\cdot 0.25/4\cdot 115\cdot 4=0.68$ kOhm

$R_2=2\cdot 2.5\cdot 0.25/0.5\cdot 30\cdot 2.1^2=19$ kOhm

a) $V_{OH}=V_{DD}=2.5V$, $V_{OL}=R_1/(R_1+R_2)=0.68/(0.68+19)\cdot 2.5=0.87$ mV

b) 1. V_{in}=Low, $I_n=0$, $P_{diss}=0$,
   2. V_{in}=High=2.5V, $I_n=I_p=(W/L)_p\cdot k_p(V_{DD}-|V_{tp}|)^2/2=133.2\ \mu A$. $P_{static}=V_{DD}\cdot I_p=2.5*133.2=333\mu W$.

c) $t_{pLH}=0.7R_pC_L=0.7*19*1=13.3$ ns; $t_{pHL}=0.7R_nC_L=0.7*0.68*1=0.476$ ns

1b19.

a) Y=!(CD(A+B))
   NMOS $(W/L)_A=(W/L)_B=(W/L)_C/2=(W/L)_D/2$; $(W/L)_C=(W/L)_D=4*3=12$; $(W/L)_A=(W/L)_B=6$
   PMOS $(W/L)_A=(W/L)_B=2(W/L)_C=2(W/L)_D$; $(W/L)_C=(W/L)_D=8/3$; $(W/L)_A=(W/L)_B=16/3$

b) tpHL: ABCD=1010 -> 1011 or 1010 -> 0111; transistor discharges the caps in all nodes of the pull-down network, before transition all caps are charged. If D were on before transition then D's drain node cap would be discharged, so tpHL would be less.
   tpLH: ABCD=1111 -> 0011; before transition all caps are charged, AB path discharges these caps.

1b20.

P(Y=1)=(1-P(A=1)P(C=1)P(D=1)) (1-P(B=1)P(C=1)P(D=1))=
=(1-0.5*0.3*0.8)(1-0.2*0.3*0.8)=0.88*0.952=0.83776
P(Y=0)=1- P(Y=1)=1-0.83776=0.16224
$P_{0-1}=P_{1-0}$= P(Y=0)*P(Y=1)= 0.1359181824=0.136
$\alpha_{sw}= P_{0-1}$
$P_{sw}= \alpha_{sw}\ VDD^2F_{clk}C_{out}=0.136*2.5^2*250*10^6*30*10^{-15}=0.659*10^{-5}W=6.59\mu W$

1b21.

Verilog Description

```
module counter_rev(clk,ce,clr,load,d,up,q,tc);
input clk, ce, clr,load,up;
input[7:0] d;
output tc;
reg tc;
output[7:0] q;
reg[7:0] q;
always @(posedge clk or posedge clr)
        begin
        if(clr==1) q<=8'b0;
        else if(load) q<=d;
                else if (ce==0)
```

```
                        q<=q;
                else if (up==1)
                        q<=q+1;
                else q<=q-1;
        end
always @(q or up)
        begin if((q==8'd255)&&(up==1))
        tc=1;
                else if((q==8'b0)&&(up==0))
                tc=1;
        else  tc=0; end

endmodule

module stimulus;
reg[7:0] d;
reg clk, ce,clr, load, up;
wire[7:0] q;
counter_rev ann(clk,ce,clr,load,d,up,q,tc);
initial begin
clk=0; clr=1; load=0;d= 8'b0;
up=1; ce=0;
#13 clr= 0;
#20 ce=1;
#100 up=0;
#50 up=1;
#2500 d=8'd127;
#100 load=1;
#100 load=0;
#600 ce=0;
#100 ce=1;
 up=0;
d=8'd255;
#20 load =1;
#20 load=0;
#100 up=0;
ce=0;
#20 d=8'd255;
#20 load=1;
#20 load=0;
#20 clr=1;
#20 clr=0;
ce=1;
d=8'd10;
#20 load=1;
#20 load=0;
# 100 $finish;
end
always #10 clk=~clk;
endmodule
```

Verilog-out

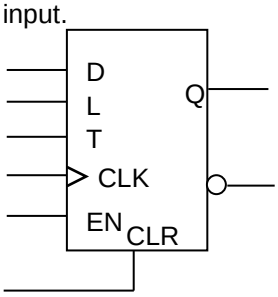
```
`include "/remote/home/stud622/VCS/dc/lib/gtech_lib.v"
module counter_rev_DW01_dec_8_0 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;
  wire   \carry[7] , \carry[6] , \carry[5] , \carry[4] , \carry[3] ,
        \carry[2] , \carry[1] ;
  assign \carry[1]  = A[0];

  GTECH_XNOR2 U1_A_1 ( .A(A[1]), .B(\carry[1] ), .Z(SUM[1]) );
  GTECH_OR2 U1_B_1 ( .A(A[1]), .B(\carry[1] ), .Z(\carry[2] ) );
  GTECH_XNOR2 U1_A_2 ( .A(A[2]), .B(\carry[2] ), .Z(SUM[2]) );
  GTECH_OR2 U1_B_2 ( .A(A[2]), .B(\carry[2] ), .Z(\carry[3] ) );
  GTECH_XNOR2 U1_A_3 ( .A(A[3]), .B(\carry[3] ), .Z(SUM[3]) );
  GTECH_OR2 U1_B_3 ( .A(A[3]), .B(\carry[3] ), .Z(\carry[4] ) );
  GTECH_XNOR2 U1_A_4 ( .A(A[4]), .B(\carry[4] ), .Z(SUM[4]) );
  GTECH_OR2 U1_B_4 ( .A(A[4]), .B(\carry[4] ), .Z(\carry[5] ) );
  GTECH_XNOR2 U1_A_5 ( .A(A[5]), .B(\carry[5] ), .Z(SUM[5]) );
  GTECH_OR2 U1_B_5 ( .A(A[5]), .B(\carry[5] ), .Z(\carry[6] ) );
  GTECH_XNOR2 U1_A_6 ( .A(A[6]), .B(\carry[6] ), .Z(SUM[6]) );
  GTECH_OR2 U1_B_6 ( .A(A[6]), .B(\carry[6] ), .Z(\carry[7] ) );
  GTECH_XNOR2 U1_A_7 ( .A(A[7]), .B(\carry[7] ), .Z(SUM[7]) );
  GTECH_NOT U6 ( .A(\carry[1] ), .Z(SUM[0]) );
endmodule

module counter_rev_DW01_inc_8_0 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;
```

```
  wire   \carry[7] , \carry[6] , \carry[5] , \carry[4] , \carry[3] ,
        \carry[2] , n1;

  GTECH_ADD_AB U1_1_1 ( .A(A[1]), .B(A[0]), .S(SUM[1]), .COUT(\carry[2] ) );
  GTECH_ADD_AB U1_1_2 ( .A(A[2]), .B(\carry[2] ), .S(SUM[2]), .COUT(\carry[3] ) );
  GTECH_ADD_AB U1_1_3 ( .A(A[3]), .B(\carry[3] ), .S(SUM[3]), .COUT(\carry[4] ) );
  GTECH_ADD_AB U1_1_4 ( .A(A[4]), .B(\carry[4] ), .S(SUM[4]), .COUT(\carry[5] ) );
  GTECH_ADD_AB U1_1_5 ( .A(A[5]), .B(\carry[5] ), .S(SUM[5]), .COUT(\carry[6] ) );
  GTECH_ADD_AB U1_1_6 ( .A(A[6]), .B(\carry[6] ), .S(SUM[6]), .COUT(\carry[7] ) );
  GTECH_OAI2N2 U5 ( .A(n1), .B(A[7]), .C(n1), .D(A[7]), .Z(SUM[7]) );
  GTECH_NOT U6 ( .A(\carry[7] ), .Z(n1) );
  GTECH_NOT U7 ( .A(A[0]), .Z(SUM[0]) );
endmodule

module counter_rev ( clk, ce, clr, load, d, up, q, tc );
  input [7:0] d;
  output [7:0] q;
  input clk, ce, clr, load, up;
  output tc;
  wire   N25, N26, N27, N28, N29, N30, N31, N32, N33, N34, N35, N36, N37, N38,
        N39, N40, N41, N42, N43, N44, N45, N46, N47, N48, N49, n28, n35, n37,
        n38, n39, n40, n41, n42, n43, n44, n45, n46, n47, n48, n49, n50;

  GTECH_FJK2S \q_reg[0]  ( .J(n28), .K(n28), .TI(N42), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[0]) );
  GTECH_FJK2S \q_reg[1]  ( .J(n28), .K(n28), .TI(N43), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[1]) );
  GTECH_FJK2S \q_reg[2]  ( .J(n28), .K(n28), .TI(N44), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[2]) );
  GTECH_FJK2S \q_reg[3]  ( .J(n28), .K(n28), .TI(N45), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[3]) );
  GTECH_FJK2S \q_reg[4]  ( .J(n28), .K(n28), .TI(N46), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[4]) );
  GTECH_FJK2S \q_reg[5]  ( .J(n28), .K(n28), .TI(N47), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[5]) );
  GTECH_FJK2S \q_reg[6]  ( .J(n28), .K(n28), .TI(N48), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[6]) );
  GTECH_FJK2S \q_reg[7]  ( .J(n28), .K(n28), .TI(N49), .TE(N25), .CP(clk),
       .CD(n35), .Q(q[7]) );
  GTECH_ZERO U48 ( .Z(n28) );
  GTECH_AOI22 U49 ( .A(n37), .B(n38), .C(n39), .D(up), .Z(tc) );
  GTECH_NAND8 U50 ( .A(q[7]), .B(q[6]), .C(q[5]), .D(q[4]), .E(q[3]), .F(q[2]),
       .G(q[1]), .H(q[0]), .Z(n39) );
  GTECH_OR8 U51 ( .A(q[0]), .B(q[1]), .C(q[2]), .D(q[3]), .E(q[4]), .F(q[5]),
       .G(q[6]), .H(q[7]), .Z(n37) );
  GTECH_NOT U52 ( .A(clr), .Z(n35) );
  GTECH_NOT U53 ( .A(n40), .Z(N49) );
  GTECH_AOI222 U54 ( .A(load), .B(d[7]), .C(N33), .D(n41), .E(N41), .F(n42),
       .Z(n40) );
  GTECH_NOT U55 ( .A(n43), .Z(N48) );
  GTECH_AOI222 U56 ( .A(d[6]), .B(load), .C(N32), .D(n41), .E(N40), .F(n42),
       .Z(n43) );
  GTECH_NOT U57 ( .A(n44), .Z(N47) );
  GTECH_AOI222 U58 ( .A(d[5]), .B(load), .C(N31), .D(n41), .E(N39), .F(n42),
       .Z(n44) );
  GTECH_NOT U59 ( .A(n45), .Z(N46) );
  GTECH_AOI222 U60 ( .A(d[4]), .B(load), .C(N30), .D(n41), .E(N38), .F(n42),
       .Z(n45) );
  GTECH_NOT U61 ( .A(n46), .Z(N45) );
  GTECH_AOI222 U62 ( .A(d[3]), .B(load), .C(N29), .D(n41), .E(N37), .F(n42),
       .Z(n46) );
  GTECH_NOT U63 ( .A(n47), .Z(N44) );
  GTECH_AOI222 U64 ( .A(d[2]), .B(load), .C(N28), .D(n41), .E(N36), .F(n42),
       .Z(n47) );
  GTECH_NOT U65 ( .A(n48), .Z(N43) );
  GTECH_AOI222 U66 ( .A(d[1]), .B(load), .C(N27), .D(n41), .E(N35), .F(n42),
       .Z(n48) );
  GTECH_NOT U67 ( .A(n49), .Z(N42) );
  GTECH_AOI222 U68 ( .A(d[0]), .B(load), .C(N26), .D(n41), .E(N34), .F(n42),
       .Z(n49) );
  GTECH_AND2 U69 ( .A(n50), .B(up), .Z(n42) );
  GTECH_AND2 U70 ( .A(n38), .B(n50), .Z(n41) );
  GTECH_NOT U71 ( .A(up), .Z(n38) );
  GTECH_OR_NOT U72 ( .A(ce), .B(n50), .Z(N25) );
  GTECH_NOT U73 ( .A(load), .Z(n50) );
  counter_rev_DW01_dec_8_0 sub_16 ( .A(q), .SUM({N33, N32, N31, N30, N29, N28, N27, N26}) );
  counter_rev_DW01_inc_8_0 add_15 ( .A(q), .SUM({N41, N40, N39, N38, N37, N36, N35, N34}) );
endmodule
```

```
module stimulus;
reg[7:0] d;
reg clk, ce,clr, load, up;
wire[7:0] q;
counter_rev ann(clk,ce,clr,load,d,up,q,tc);
initial begin
clk=0; clr=1; load=0;d= 8'b0;
up=1; ce=0;
#13 clr= 0;
#20 ce=1;
#100 up=0;
#50 up=1;
#2500 d=8'd127;
#100 load=1;
#100 load=0;
#600 ce=0;

#100 ce=1;
 up=0;
d=8'd255;
#20 load =1;
#20 load=0;

#100 up=0;
ce=0;
#20 d=8'd255;
#20 load=1;
#20 load=0;
#20 clr=1;
#20 clr=0;
ce=1;
d=8'd10;
#20 load=1;
#20 load=0;
# 100 $finish;
end
always #10 clk=~clk;
endmodule
```

Constructing a counter circuit diagram based on T Flip-Flop

To construct a circuit diagram use T flip-flops with asynchronous reset, synchronous loading and enable input.



T- toggling enable input
L – load enable
D – data input
CCLK– clock input
EN - clock enable input
CLR – asynchronous reset

Truth table of FF:

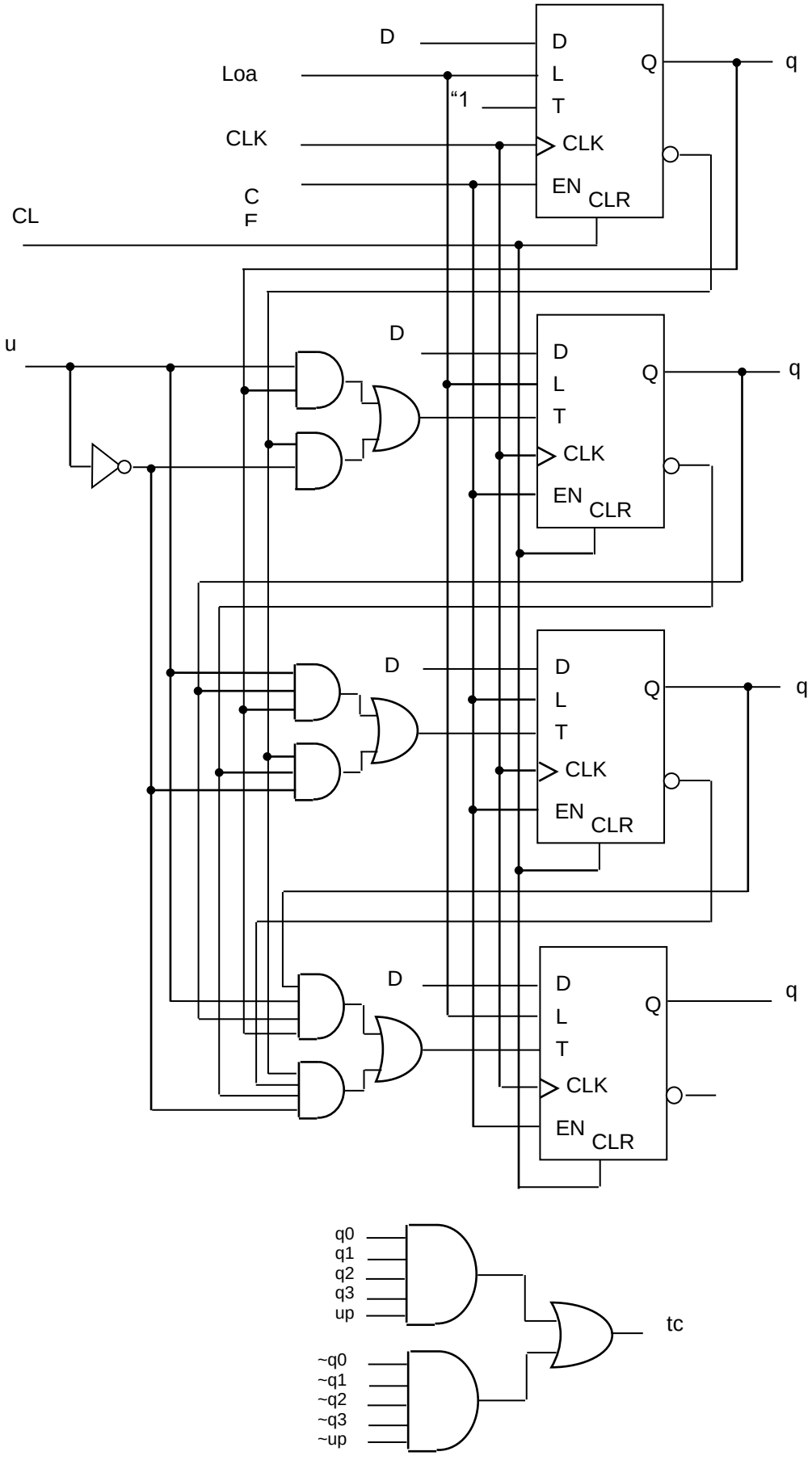
CLR	EN	L	D	T	CLK	Q	Mode
1	x	x	x	x	x	0	Reset
0	x	1	0	x	↑	0	Syn. „0” writing
0	x	1	1	x	↑	1	Syn. „0” writing
0	0	0	x	x	x	Q_{last}	Hold
0	1	0	x	0	↑	Q_{last}	Hold
0	1	0	x	0	x	Q_{last}	Hold
0	1	0	x	1	↑	$\sim Q_{last}$	Switching

Definition of reversive counter's excitation function

Present_state				Input	Next_state				Excitation Function			
q3	q2	q1	q0	up	q3	q2	q1	q0	t3	t2	t1	t0
0	0	0	0	0	1	1	1	1	1	1	1	1
				1	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1
				1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	0	0	1	0	0	1	1
				1	0	0	1	1	0	0	0	1
0	0	1	1	0	0	0	1	0	0	0	0	1
				1	0	1	0	0	0	1	1	1
0	1	0	0	0	0	0	1	1	0	1	1	1
				1	0	1	0	1	0	0	0	1
0	1	0	1	0	0	1	0	0	0	0	0	1
				1	0	1	1	0	0	0	1	1
0	1	1	0	0	0	1	0	1	0	0	1	1
				1	0	1	1	1	0	0	0	1
0	1	1	1	0	0	1	1	0	0	0	0	1
				1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
				1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	0	0	0	0	0	1
				1	1	0	1	0	0	0	1	1
1	0	1	0	0	1	0	0	1	0	0	1	1
				1	1	0	1	1	0	0	0	1
1	0	1	1	0	1	0	1	0	0	0	0	1
				1	1	1	0	0	0	1	1	1
1	1	0	0	0	1	0	1	1	0	1	1	1
				1	1	1	0	1	0	0	0	1
1	1	0	1	0	1	1	0	0	0	0	0	1
				1	1	1	1	0	0	0	1	1
1	1	1	0	0	1	1	0	1	0	0	1	1
				1	1	1	1	1	0	0	0	1
1	1	1	1	0	1	1	1	0	0	0	0	1
				1	0	0	0	0	1	1	1	1

t0 = 1; t1 = q0·up + ~q0·~up;
t2 = q0·q1·up + ~q0·~q1·~up;
t3 = q0·q1·q2·up + ~q0·~q1·~q2·~up;
tc= q0·q1·q2· q3·up + ~q0·~q1·~q2·~q3·~up;

Based on the obtained results, construct the counter circuit.



1b22.

Verilog Description

```
module counter_dec(clk,ce,reset,load,d,q,tc);
input clk, ce, reset,load;
input[3:0] d;
output tc;
reg tc;
output[3:0] q;
reg[3:0] q;
always @(posedge clk)
begin
if(reset==1) q<=4'b0;
else if(load) begin if (d>= 4'd10) q<=4'b0;
else q<=d; end
else if ((ce==1)&&(q==4'd9))  q <= 4'b0;
else if(ce==1)  q<=q+1;
else q<=q;
end

always @(q)

if(q==4'd9) tc=1;
else  tc=0;

endmodule

module stimulus;
reg[3:0] d;
reg clk, ce,reset, load;
wire[3:0] q;
counter_dec ann(clk,ce,reset,load,d,q,tc);
initial begin
clk=0; reset=1; load=0;d= 4'd5;
 ce=0;
#13 reset= 0;
#20 ce=1;
#90 ce=0;
# 100 load=1;
#20 load=0;
#10 ce=0;
#10 d=4'd12;
load=1;
#32 d=4'd9;

#50 ce=1;
#100 load=1;
load=1;
d=8'b0;
#10 load=0;
# 100 $finish;
end
always #5 clk=~clk;
endmodule
```

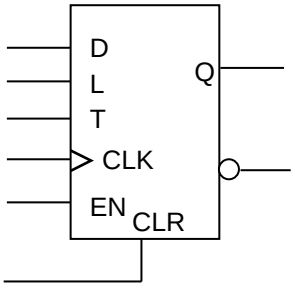
Verilog-out

```
include "/remote/home/stud622/VCS/dc/lib/gtech_lib.v"
module counter_dec ( clk, ce, reset, load, d, q, tc );
  input [3:0] d;
  output [3:0] q;
  input clk, ce, reset, load;
  output tc;
  wire   N8, N31, N32, N33, N34, n16, n17, n27, n31, n32, n33, n34, n35, n36,
        n37, n38, n39, n40, n41, n42, n43, n44;

  GTECH_FJK1S \q_reg[3]  ( .J(n27), .K(n27), .TI(N34), .TE(N8), .CP(clk), .Q(
      q[3]), .QN(n43) );
  GTECH_FJK1S \q_reg[2]  ( .J(n27), .K(n27), .TI(N33), .TE(N8), .CP(clk), .Q(
      q[2]), .QN(n16) );
  GTECH_FJK1S \q_reg[1]  ( .J(n27), .K(n27), .TI(N32), .TE(N8), .CP(clk), .Q(
      q[1]), .QN(n17) );
  GTECH_FJK1S \q_reg[0]  ( .J(n27), .K(n27), .TI(N31), .TE(N8), .CP(clk), .Q(
      q[0]), .QN(n44) );
  GTECH_ZERO U23 ( .Z(n27) );
  GTECH_OR3 U24 ( .A(load), .B(reset), .C(ce), .Z(N8) );
  GTECH_OAI2N2 U25 ( .A(n31), .B(n32), .C(d[3]), .D(n33), .Z(N34) );
  GTECH_OAI2N2 U26 ( .A(n34), .B(q[3]), .C(n34), .D(q[3]), .Z(n31) );
  GTECH_AND2 U27 ( .A(n35), .B(q[2]), .Z(n34) );
```

```
  GTECH_OAI2N2 U28 ( .A(n36), .B(n32), .C(n33), .D(d[2]), .Z(N33) );
  GTECH_OAI2N2 U29 ( .A(n35), .B(q[2]), .C(n35), .D(q[2]), .Z(n36) );
  GTECH_AND_NOT U30 ( .A(q[1]), .B(n37), .Z(n35) );
  GTECH_OAI2N2 U31 ( .A(n38), .B(n32), .C(n33), .D(d[1]), .Z(N32) );
  GTECH_XOR2 U32 ( .A(q[1]), .B(n37), .Z(n38) );
  GTECH_OAI2N2 U33 ( .A(q[0]), .B(n32), .C(d[0]), .D(n33), .Z(N31) );
  GTECH_AND3 U34 ( .A(n39), .B(n40), .C(load), .Z(n33) );
  GTECH_NOT U35 ( .A(reset), .Z(n40) );
  GTECH_OAI21 U36 ( .A(d[1]), .B(d[2]), .C(d[3]), .Z(n39) );
  GTECH_OR4 U37 ( .A(n41), .B(tc), .C(load), .D(reset), .Z(n32) );
  GTECH_NOR4 U38 ( .A(n42), .B(n37), .C(q[1]), .D(q[2]), .Z(tc) );
  GTECH_NOT U39 ( .A(q[0]), .Z(n37) );
  GTECH_NOT U40 ( .A(q[3]), .Z(n42) );
  GTECH_NOT U41 ( .A(ce), .Z(n41) );
endmodule

module stimulus;
reg[3:0] d;
reg clk, ce,reset, load;
wire[3:0] q;
counter_dec ann(clk,ce,reset,load,d,q,tc);
initial begin
clk=0; reset=1; load=0;d= 4'd5;
 ce=0;
#13 reset= 0;
#20 ce=1;
#90 ce=0;
# 100 load=1;
#20 load=0;
#10 ce=0;
#10 d=4'd12;
load=1;
#32 d=4'd9;

#50 ce=1;
#100 load=1;
load=1;
d=8'b0;
#10 load=0;
# 100 $finish;
end
always #5 clk=~clk;
endmodule
```

Constructing a counter circuit diagram based on T Flip-Flop

To construct a circuit diagram use T flip-flops with asynchronous reset, synchronous loading and enable input.



T- toggling enable input
L – load enable
D – data input
CLK– clock input
EN - clock enable input
CLR – synchronous reset

Truth table of FF:

CLR	EN	L	D	T	CLK	Q	Mode
1	x	x	x	x	↑	0	Reset
1	x	1	0	x	↑	0	Syn. „0” writing
1	x	1	1	x	↑	1	Syn. „0” writing
1	0	0	x	x	x	Q_{last}	Hold
1	1	0	x	0	↑	Q_{last}	Hold
1	1	0	x	0	x	Q_{last}	Hold

1	1	0	x	1	↑	~Q_{last}	Switching

Definition of binary-coded decimal counter's excitation function:

q3	q2	q1	q0	t3	t2	t1	t0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	1	1	1
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	1
0	1	1	0	0	0	0	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1
1	0	0	1	1	0	0	1

Exitation Function's Minimization using Karnaugh Maps

t3

q3q2 \ q1q0	00	01	11	10
00				
01			1	
11	–	–	–	–
10		1	–	–

t2

q3q2 \ q1q0	00	01	11	10
00			1	
01			1	
11	–	–	–	–
10			–	–

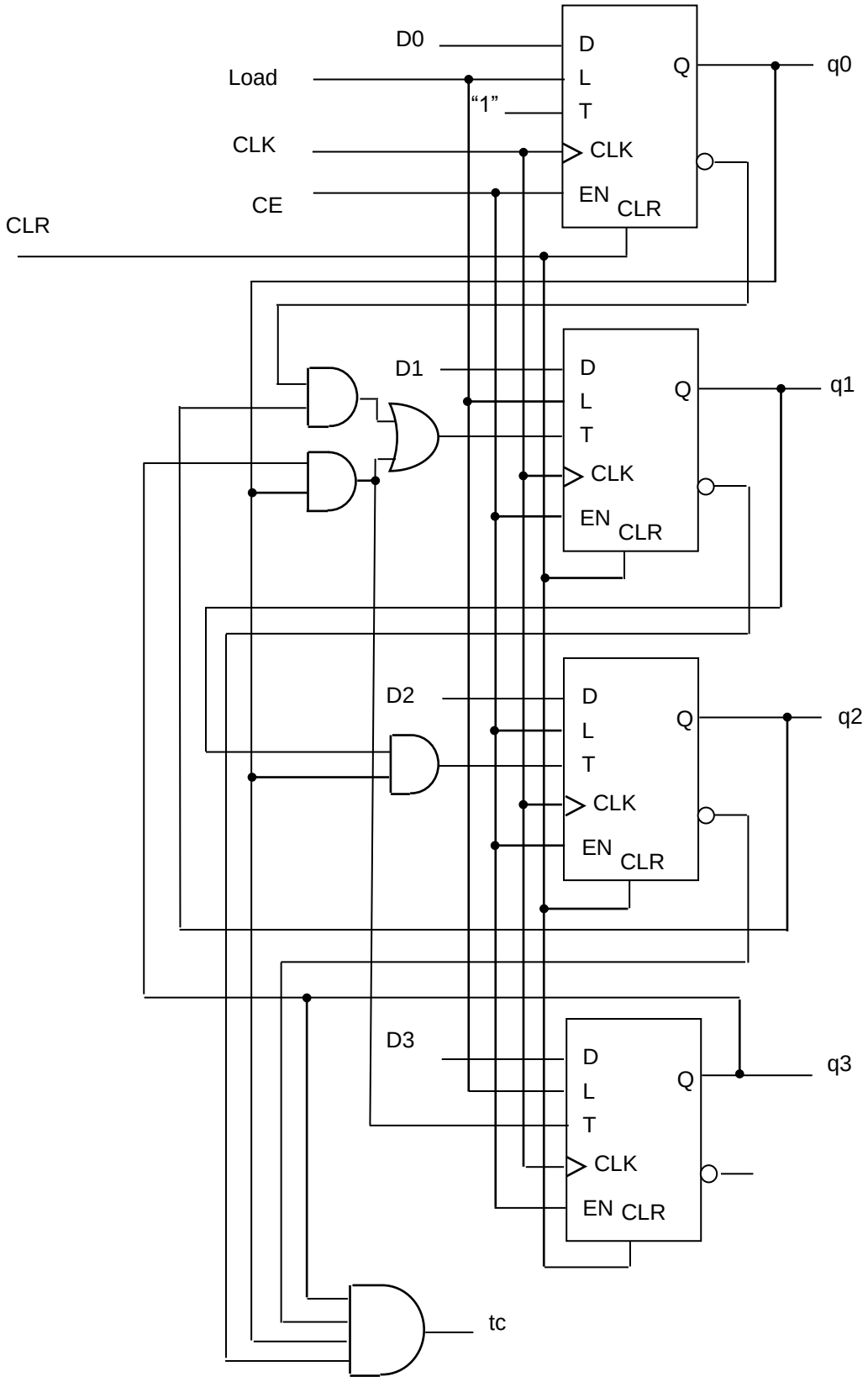
t1

q3q2 \ q1q0	00	01	11	10
00			1	1
01		1	1	
11	–	–		–
10			–	–

t0 = 1
t1 = q0·q3+~q0·q2
t2 = q0·q1
t3 = q0·q3

t0 = 1
t1 = q0·q3+~q0·q3
t2 = q0·q1
t3 = q0·q3

Circuit diagram is constructed based on the obtained results.

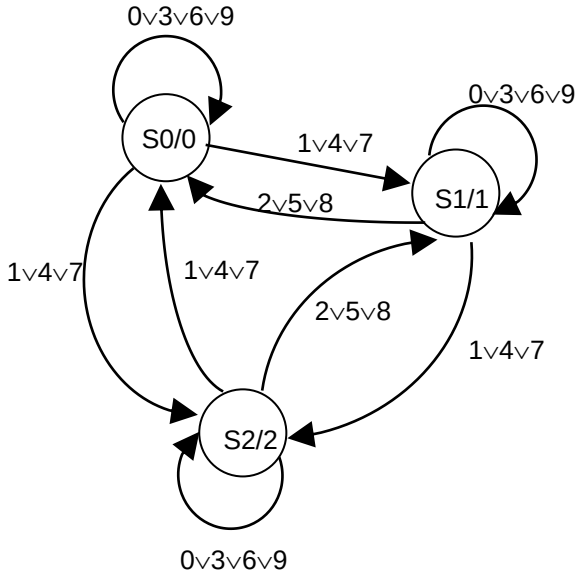


1b23.

Creation of State Transition Graph of FSM

The digits of entering decimal number are given on the entries of FSM sequentially.
The remainder of division of a decimal number by 3 is equal to the remainder of division of the sum of decimal digits of this number by 3.
FSM is given by means of the following five sets: A = { X, Y, S, δ , λ}, where:
X = {X1, X2 . . . XM} – set of input symbols;
Y = {Y1, Y2 . . . YN} – set of output symbols;
S = {S0, S1 . . . SK-1} – set of internal states of FSM;
δ – next state (transition) function,
λ - output function.

The considered FSM has 3 states S = {S0,S1,S2},
where, S0 – the remainder equal to 0,S1 – the remainder equal to 1,S2 – the remainder equal to 2.
X = {0,1,2,3,4,5,6,7,8,9}
Y = {0,1,2}
S = {S0,S1,S2}



Verilog Description of FSM

```
module fsm_remainder(in,clk,reset,out);
input[3:0] in;
input clk, reset;
output[1:0] out;
reg [1:0] out;
reg[1:0] state, next_state;
parameter S0=2'b00, S1=2'b01, S2=2'b10;
always @(posedge clk or negedge reset)
if(!reset) state <= S0;
else state<=next_state;
always @(in or state)
begin
case(state)
S0: case(in)
4'd0,4'd3,4'd6,4'd9: next_state=S0;
4'd1, 4'd4, 4'd7:    next_state=S1;
4'd2, 4'd5, 4'd8:    next_state=S2;
default: next_state=S0;
endcase
S1: case(in)
4'd0,4'd3,4'd6,4'd9:  next_state=S1;
4'd1, 4'd4, 4'd7:     next_state=S2;
4'd2, 4'd5, 4'd8:     next_state=S0;
default: next_state=S0;
endcase
```

```
S2: case(in)
4'd0,4’d3,4’d6,4’d9: next_state=S2;
4'd1, 4’d4, 4’d7:     next_state=S0;
4'd2, 4’d5, 4’d8:     next_state=S1;
default: next_state=S0;
endcase
default: next_state=S0;
endcase
end
always @(state)
if(state==S0) out=2'b00;
else if (state==S1) out = 2'b01;
else if (state ==S2) out = 2'b10;
else out=2'bxx;
endmodule

module stimulus;
reg[3:0] in;
wire[1:0] out;
reg clk, reset;
fsm_remainder  ann(in,clk,reset,out);
initial begin
clk=0;
reset=1;
#10 reset = 0;
in=0;
#13 reset = 1;
#10 in = 4'd0;
#10 in = 4'd2;
#10 in = 4'd4;
#10 in = 4'd3;
#10 in = 4'd5;
#10 in = 4'd9;
#10 in = 4'd7;
#10 in = 4'd8;
#10 in = 4'd1;
#10 in = 4'd7;
#10 $finish;
end
always #5 clk = ~clk;
endmodule
```

Verilog-out

```
`include "/remote/home/stud622/VCS/dc/lib/gtech_lib.v"
module fsm_remainder ( in, clk, reset, out );
  input [3:0] in;
  output [1:0] out;
  input clk, reset;
  wire   n25, n26, n27, n28, n29, n30, n31, n32, n33, n34, n35, n36, n37;
  wire   [1:0] state;
  wire   [1:0] next_state;
  GTECH_FD2 \state_reg[0]  ( .D(next_state[0]), .CP(clk), .CD(reset), .Q(
        state[0]) );
  GTECH_FD2 \state_reg[1]  ( .D(next_state[1]), .CP(clk), .CD(reset), .Q(
        state[1]) );
  GTECH_NOT U30 ( .A(n25), .Z(next_state[1]) );
  GTECH_AOI222 U31 ( .A(out[0]), .B(n26), .C(n27), .D(n28), .E(out[1]), .F(n29), .Z(n25) );
  GTECH_NOT U32 ( .A(n30), .Z(next_state[0]) );
  GTECH_AOI222 U33 ( .A(out[1]), .B(n28), .C(n27), .D(n26), .E(out[0]), .F(n29), .Z(n30) );
  GTECH_MUX2 U34 ( .A(n31), .B(n32), .S(in[0]), .Z(n29) );
  GTECH_NOR2 U35 ( .A(n33), .B(state[1]), .Z(out[0]) );
  GTECH_NOT U36 ( .A(state[0]), .Z(n33) );
  GTECH_MUX2 U37 ( .A(n34), .B(n31), .S(in[0]), .Z(n26) );
  GTECH_NOR2 U38 ( .A(in[3]), .B(n35), .Z(n31) );
  GTECH_AOI2N2 U39 ( .A(in[1]), .B(in[2]), .C(in[1]), .D(in[2]), .Z(n35) );
  GTECH_NOR2 U40 ( .A(state[0]), .B(state[1]), .Z(n27) );
  GTECH_MUX2 U41 ( .A(n32), .B(n34), .S(in[0]), .Z(n28) );
  GTECH_NOR3 U42 ( .A(in[1]), .B(in[3]), .C(n36), .Z(n34) );
  GTECH_NOT U43 ( .A(in[2]), .Z(n36) );
  GTECH_NOR2 U44 ( .A(in[2]), .B(n37), .Z(n32) );
  GTECH_XNOR2 U45 ( .A(in[3]), .B(in[1]), .Z(n37) );
  GTECH_AND_NOT U46 ( .A(state[1]), .B(state[0]), .Z(out[1]) );
endmodule

module stimulus;
reg[3:0] in;
wire[1:0] out;
reg clk, reset;
fsm_remainder  ann(in,clk,reset,out);
```

```
initial begin
clk=0;
reset=0;
in=0;
#23 reset = 1;
#20 in = 4'd0;
#20 in = 4'd2;
#20 in = 4'd4;
#20 in = 4'd3;
#20 in = 4'd5;
#20 in = 4'd9;
#20 in = 4'd7;
#20 in = 4'd8;
#20 in = 4'd1;
#20 in = 4'd7;
#20 $finish;
end
always #10 clk = ~clk;
endmodule
```

Synthesis of FSM Using JK Flip-Flops

1. Definition of input and output signals

To code decimal digits $n = \lceil \log_2 10 \rceil = 4$ input variables are required, as x3, x2, x1, x0.

Binary-coded decimal digits:

Decimal digit	x3 x2 x1 x0
“0”	0 0 0 0
“1”	0 0 0 1
“2”	0 0 1 0
“3”	0 0 1 1
“4”	0 1 0 0
“5”	0 1 0 1
“6”	0 1 1 0
“7”	0 1 1 1
“8”	1 0 0 0
“9”	1 0 0 1

Y = {0, 1, 2}.

To code output signals two variables are required, as y1, y0.

Output	y1 y0
“0”	0 0
“1”	0 1
“2”	1 0

So, FSM has 4 inputs and 2 outputs.

2. State assignment

The number of required state variables k is defined as follows:

$3 \leq k \leq \log_2 3$. Accept k=2.

S0 – 00

S1 – 01

S2 – 10

Unused state – 00 (solution of minimal-value)

Definition of excitation function

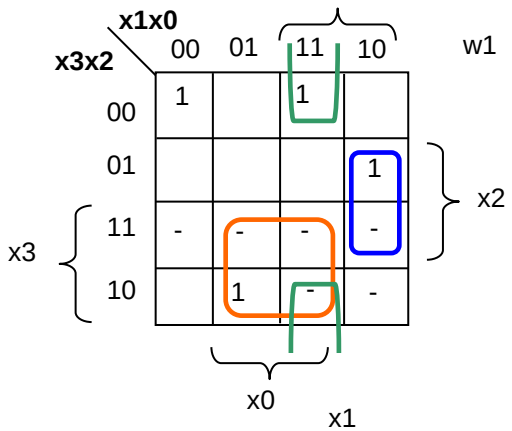
Transition	J K
0 - 0	0 x
0 - 1	1 x
1 - 0	x 1
1 - 1	x 0

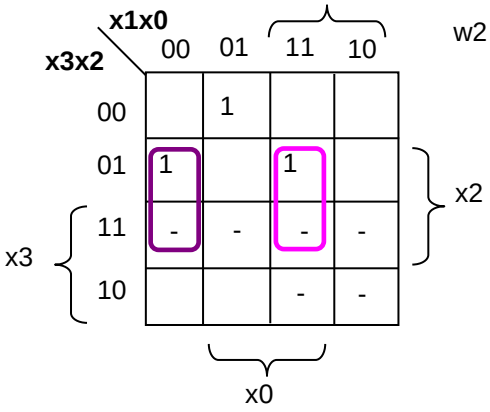
State and output table

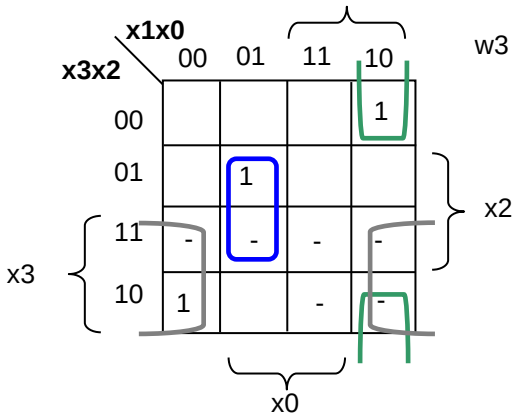
Present_state	Output	Input	Next_State	Excitation Functions
q1 q0	y1 y0	X	q1 q0	j1 k1 j0 k0
0 0	0 0	0v3v6í9	0 0	0 - 0 -
		1í4í7	0 1	0 - 1 -
		2□5□8	1 0	1 - 0 -
0 1	0 1	0v3v6v9	0 1	0 - - 0
		1v4v7	1 0	1 - - 1
		2v5v8	0 0	0 - - 1

1 0	1 0	0v3v6v9	1 0	- 0 0 -
		1v4v7	0 0	- 1 0 -
		2v5v8	0 1	- 1 1 -

Excitation functions depend on 6 variables: q1,q2,x0,x1,x2,x3.
To simplify the process of designing w1, w2, w3 extra variables are inserted:
0v3v6v9 - w1;
1v4v7 - w2;
2v5v8 - w3;
Karnaugh maps for w1,w2,w3.







w1 = ~x3·~x2·~x1·~x0 + ~x2·x1·x0 + x2·x1·~x0 + x3·x0
w2 = ~x3·~x2·~x1·x0 + x2·~x1·~x0 +x2·x1·x0
w3 = x3·~x0 + x2·~x1·x0 + ~x2·x1·x0

Definition of j1,k1,j2,k2 excitation functions as function of w1,w2,w3,q1,q0.
j1=w1f1 +w2f2+w3f3; k1=w1g1+w2g2+w3g3
j0=w1p1+w2p2+w3p3, k0=w1t1+w2t2+w3t3, where f1…f3,g1,…g3, p1…p3, t1... t3 depend on q1,q2 variables.

As follows from the above table, f1 and g1 are equal to 0.

Maps for definition f2,g2,p2,t2
(factors for w2)

j1

q1 \ q0	0	1
0	0	1
1	-	-

f2 = q2

k1

q1 \ q0	0	1
0	-	-
1	1	-

g2=1

J0

q1 \ q0	0	1
0	1	-
1	0	-

p2=1

K0

q1 \ q0	0	1
0	-	1
1	-	-

t2=1

Maps for definition f3,g3,p3,t3
(factors for w3)

J1

q1 \ q0	0	1
0	1	0
1	-	-

f3=~q2

k1

q1 \ q0	0	1
0	-	-
1	1	-

g3=1

J0

q1 \ q0	0	1
0	0	-
1	1	-

p3=q1

K0

q1 \ q0	0	1
0	-	1
1	-	-

t3=1

So,
j1=w2q2 + w3~q2;
k1 = w2 + w3;
j0=w2~q1+ w3q1;
k0=w2 + w3;

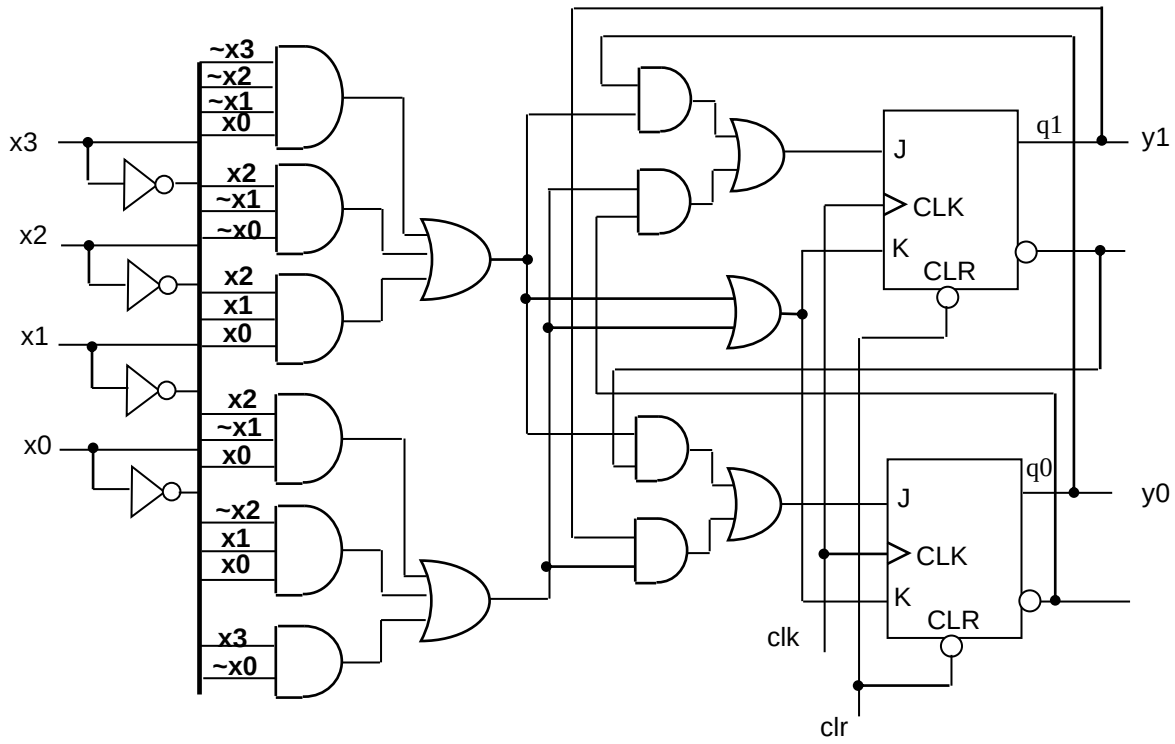
Maps for defining y1, y0

q1 \ q0	0	1
0	0	0
1	1	-

q1 \ q0	0	1
0	0	1
1	0	-

y1=q1; y0=q0;

FSM circuit diagram



1b24.

Creation of State Transition Graph of FSM

FSM is given by means of the following five sets: A = { X, Y, S, δ , λ}, where X = {X1, X2 . . . XM} – set of input symbols;

Y = {Y1, Y2 . . . YN} – set of output symbols;

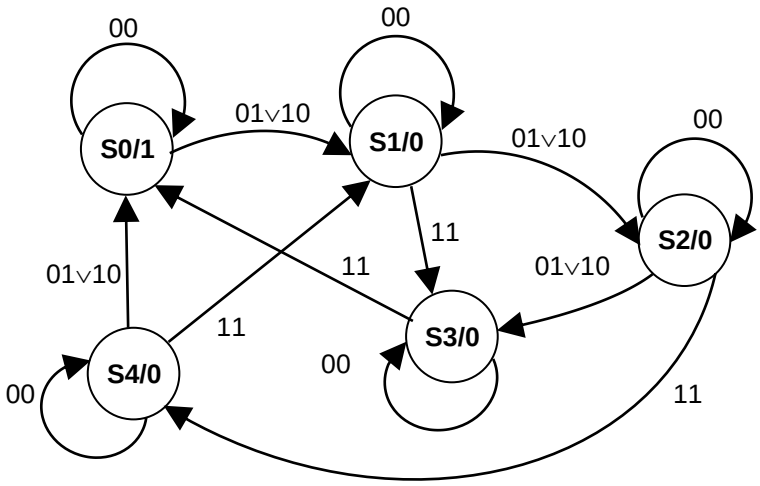
S = {S0, S1 . . . SK-1} – set of internal states of FSM;

δ – next state (transition) function,

λ - output function

X={00,01,10,11}

Y={0,1}



S0 – got zero 1s (modulo 5)
S1 – got one 1 (modulo 5)
S2 – got two 1s (modulo 5)
S3 – got three 1s (modulo 5)
S4 – got four 1s (modulo 5)

Verilog Description of FSM

```
module moore_countmod5(data,clock,reset,out);
        input reset, clock;
        input[1:0] data;
        output out;
        reg out;
        reg [2:0] state, next_state;
        parameter st0 = 3'b000, st1 = 3'b001, st2 = 3'b010, st3=3'b011, st4=3'b100;
        //FSM register
                always @(posedge clock or negedge reset)
                begin: statereg
                        if(!reset) //asynchronous reset
                        state <= st0;
                        else state <= next_state;
                        end //statereg
        //FSM next_state logic
        always @(state or data)
                begin: fsm
                case (state)
                st0: case (data)
                        2'b00: next_state = st0;
                        2'b01,2'b10: next_state = st1;
                        2'b11: next-state = st2;
                        default: next_state = st0;
                        endcase
                st1:case(data)
                        2'b00: next_state =st1;
                        2'b01, 2'b10: next_state=st2;
                        2'b11: next_state = st3;
                        default: next_state = st0;
                        endcase
                st2: case(data)
                        2'b00: next_state = st2;
```

```
                    2'b01, 2'b10: next_state=st3;
                    2'b11: next_state = st4;
                    default: next_state = st0;
                    endcase
            st3: case(data)
                    2'b00: next_state = st3;
                    2'b01, 2'b10: next_state=st4;
                    2'b11: next_state = st0;
                    default: next_state = st0;
                    endcase
            st4: case(data)
                    2'b00: next_state = st4;
                    2'b01, 2'b10: next_state=st0;
                    2'b11: next_state = st1;
                    default: next_state = st0;
                    endcase
            default: next_state = st0;
            endcase
            end//fsm
        //Moore output definition using pres_state only
            always @(state)
            begin: def_out
            if (state == st0)
            out = 1'b1;
            else out = 1'b0;
            end//def_out
            endmodule

        module test_bench_moore;
        wire out;
        reg clock, reset;
        reg[1:0] data;
moore_countmod5 ann(data,clock,reset,out);
        initial begin
        reset = 0;
        clock = 0;
        data = 2'b00;
        #13 reset = 1;
        #10 data = 2'b01;
        #10 data = 2'b11;
        #10 data = 2'b10;
        #10 data = 2'b11;
        #10 data = 2'b00;
        #10 data = 2'b11;
        #10 data = 2'b10;
        #10 data = 2'b11;
        #10 data = 2'b00;
        #10 data = 2'b10;
        #10 data = 2'b10;
        #20 reset = 0;
        #50 $finish;
        end
always #5 clock =~clock;
endmodule
```

Verilog-out

```
`include "/remote/home/stud622/VCS/dc/lib/gtech_lib.v"
module moore_countmod5 ( data, clock, reset, out );
  input [1:0] data;
  input clock, reset;
  output out;
  wire   n29, n30, n31, n32, n33, n34, n35, n36, n37, n38, n39, n40, n41;
  wire   [2:0] state;
  wire   [2:0] next_state;
  GTECH_FD2 \state_reg[2]  ( .D(next_state[2]), .CP(clock), .CD(reset), .Q(
       state[2]), .QN(n29) );
  GTECH_FD2 \state_reg[1]  ( .D(next_state[1]), .CP(clock), .CD(reset), .Q(
       state[1]), .QN(n31) );
  GTECH_FD2 \state_reg[0]  ( .D(next_state[0]), .CP(clock), .CD(reset), .Q(
       state[0]), .QN(n30) );
  GTECH_AND3 U20 ( .A(n32), .B(n33), .C(n34), .Z(out) );
  GTECH_MUX2 U21 ( .A(n35), .B(n36), .S(state[2]), .Z(next_state[2]) );
  GTECH_AND2 U22 ( .A(n37), .B(n32), .Z(n36) );
  GTECH_AND2 U23 ( .A(n38), .B(state[1]), .Z(n35) );
  GTECH_AND2 U24 ( .A(n39), .B(n33), .Z(next_state[1]) );
  GTECH_MUX2 U25 ( .A(n38), .B(n37), .S(state[1]), .Z(n39) );
  GTECH_OAI22 U26 ( .A(data[1]), .B(data[0]), .C(state[0]), .D(n40), .Z(n37) );
  GTECH_OAI2N2 U27 ( .A(n40), .B(n34), .C(data[1]), .D(data[0]), .Z(n38) );
  GTECH_NOT U28 ( .A(state[0]), .Z(n34) );
```

```
  GTECH_OA21 U29 ( .A(n33), .B(n32), .C(n41), .Z(next_state[0]) );
  GTECH_XNOR2 U30 ( .A(n40), .B(state[0]), .Z(n41) );
  GTECH_XNOR2 U31 ( .A(data[1]), .B(data[0]), .Z(n40) );
  GTECH_NOT U32 ( .A(state[1]), .Z(n32) );
  GTECH_NOT U33 ( .A(state[2]), .Z(n33) );
endmodule

module test_bench_moore;
        wire out;
        reg clock, reset;
        reg[1:0] data;
moore_countmod5 ann(data,clock,reset,out);
        initial begin
        reset = 0;
        clock = 0;
        data = 2'b00;
        #23 reset = 1;
        #20 data = 2'b01;
        #20 data = 2'b11;
        #20 data = 2'b10;
        #20 data = 2'b11;
        #20 data = 2'b00;
        #20 data = 2'b11;
        #20 data = 2'b10;
        #20 data = 2'b11;
        #20 data = 2'b00;
        #20 data = 2'b10;
        #20 data = 2'b10;
        #40 reset = 0;
        #50 $finish;
        end
always #10 clock =~clock;
endmodule
```

Synthesis of FSM using D flip-flops

1. State Assignment (first example)

Number of flip-flops: n=⌈log$_2$5⌉ = 3.

S0 – 000

S1 – 001

S2 – 010

S3 – 101

S4 – 100

FSM inputs are designated as x1, x2.

FSM output is designated as y.

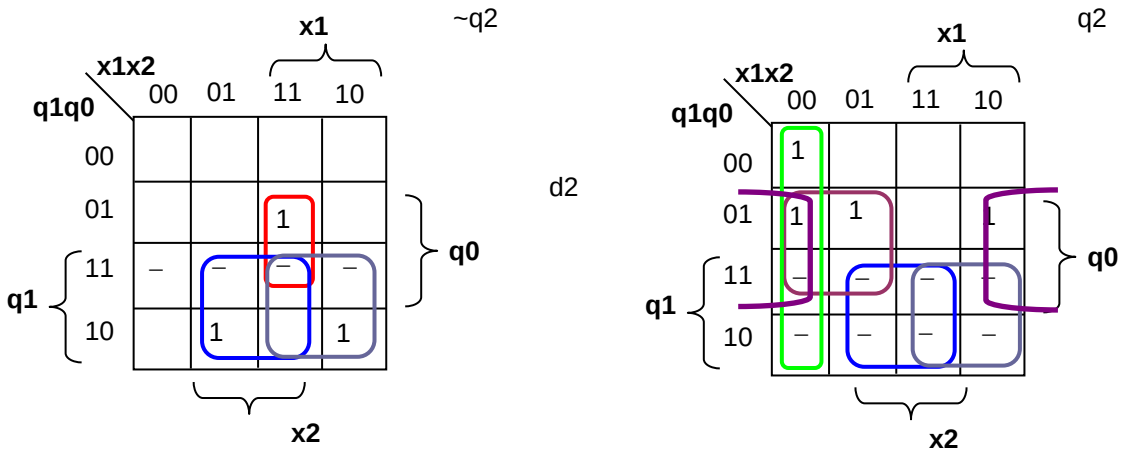
2. Transition and output table

Present_state		Input	Next_state	Excitation Functions
q2 q1 q0	y	x1 x2	q2 q1 q0	d2 d1 d0
0 0 0	1	00	0 0 0	0 0 0
		01v10	0 0 1	0 0 1
		11	0 1 0	0 1 0
0 0 1	0	00	0 0 1	0 0 1
		01v10	0 1 0	0 1 0
		11	1 0 1	1 0 1
0 1 0	0	00	0 1 0	0 1 0
		01v10	1 0 1	1 0 1
		11	1 0 0	1 0 0
1 0 1	0	00	1 0 1	1 0 1
		01v10	1 0 0	1 0 0
		11	0 0 0	0 0 0
1 0 0	0	00	1 0 0	1 0 0
		01v10	0 0 0	0 0 0
		11	0 0 1	0 0 1

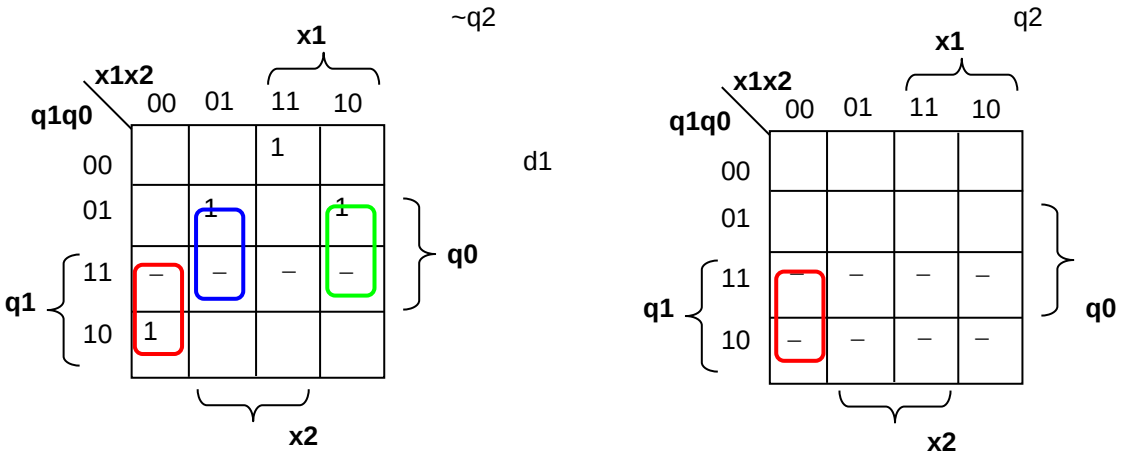
3. Minimization of Excitation Functions

d2, d1, d0 depend on 5 variables: q2,q1,q0,x1,x2.

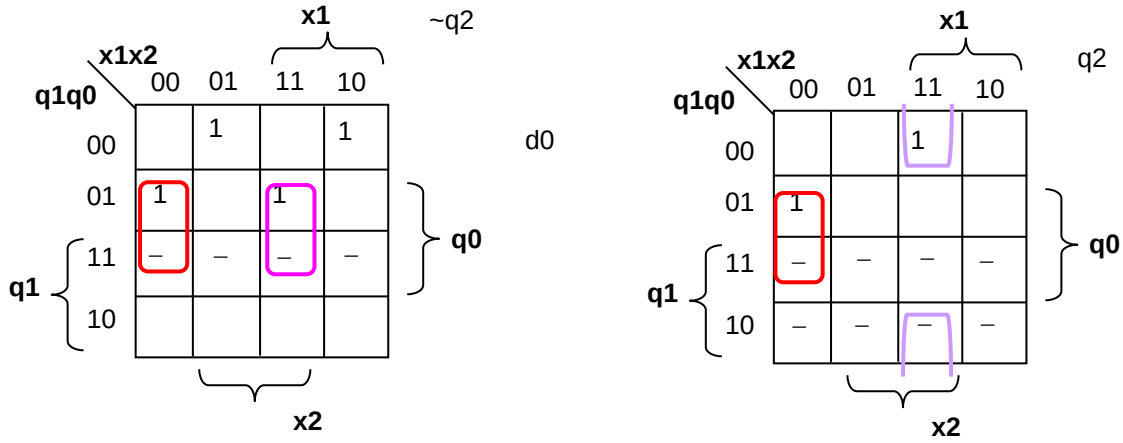
Unused states: 011, 110, 111. (solution of minimal-value)



d2=q1·x2 +q1·x1+~q2q0x1x2+q2~x1~x2+q0q2~x1+q2q0~x2



d1=q1~x1~x2+q0~q2~x1x2+q0~q2x1~x2+~q2~q1~q0x1x2



d0=q0~x1~x2+q0~q2x1x2+~q0~q1~q2~x1x2+~q0~q1~q2x1~x2+~q0q2x1x2

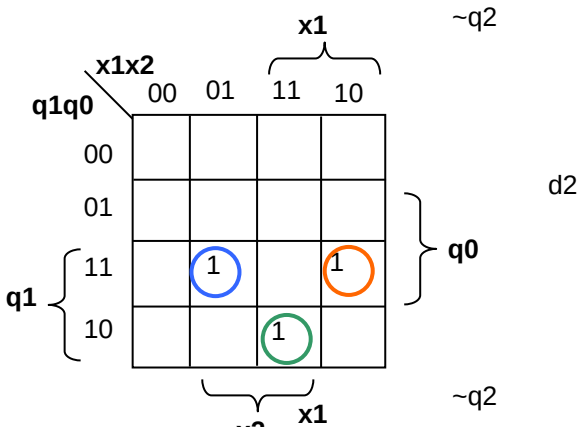
The number of inputs of gates is equal to 69.

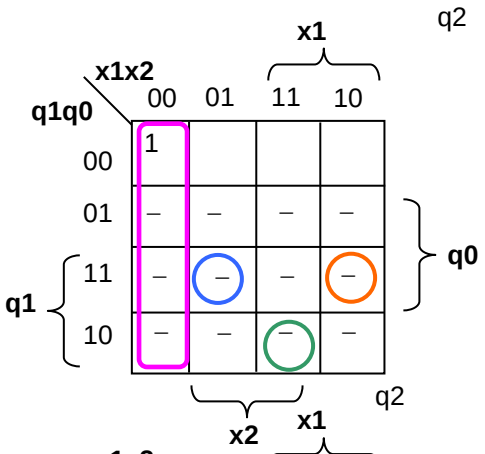
4. The second example of states assignment using D flip-flops
S0 – 000, S1 – 001, S2 – 010, S3 - 011, S4 – 100.

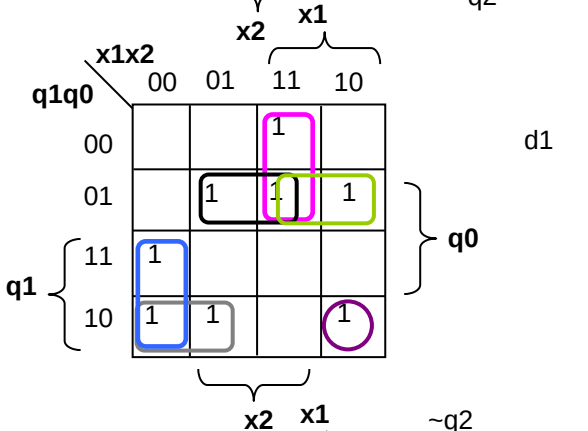
Unused states. 101, 110, 111 (minimal-value solution)

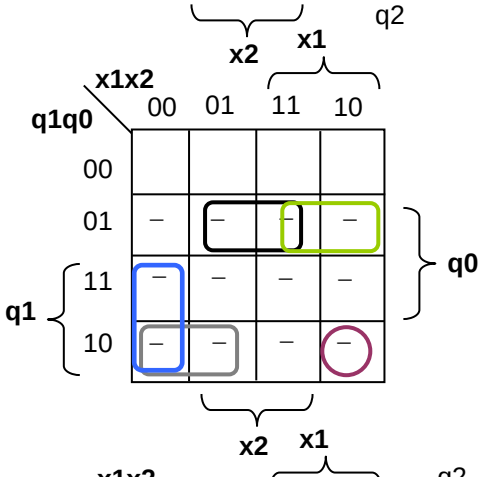
Present_state		Input	Next_state	Excitation Functions	Excitation Functions
q2 q1 q0	y	x1 x2	q2 q1 q0	t2 t1 t0	d2 d1 d0
0 0 0	1	00	0 0 0	0 0 0	0 0 0
		01v10	0 0 1	0 0 1	0 0 1
		11	0 1 0	0 1 0	0 1 0
0 0 1	0	00	0 0 1	0 0 0	0 0 1
		01v10	0 1 0	0 1 1	0 1 0
		11	0 1 1	0 1 0	0 1 1
0 1 0	0	00	0 1 0	0 0 0	0 1 0
		01v10	0 1 1	0 0 1	0 1 1
		11	1 0 0	1 1 0	1 0 0
1 0 1	0	00	0 1 1	0 0 0	0 1 1
		01v10	1 0 0	1 0 0	1 0 0
		11	0 0 0	0 1 1	0 0 0
1 0 0	0	00	1 0 0	0 0 0	1 0 0
		01v10	0 0 0	1 0 0	0 0 0
		11	0 0 1	1 0 1	0 0 1

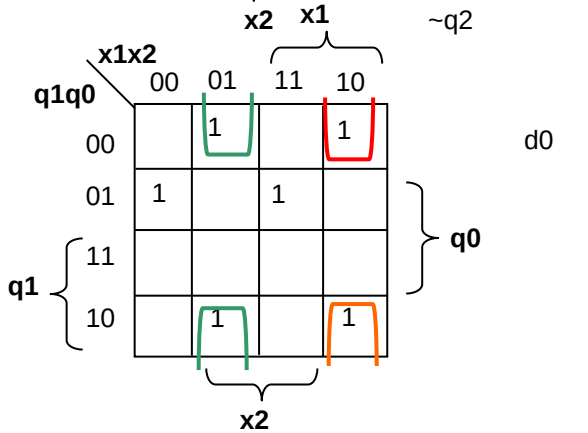
Minimization of Excitation Functions

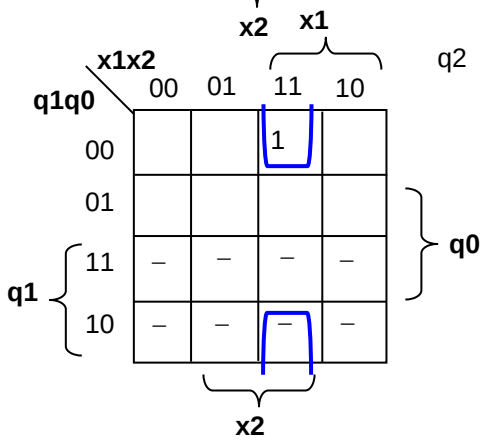








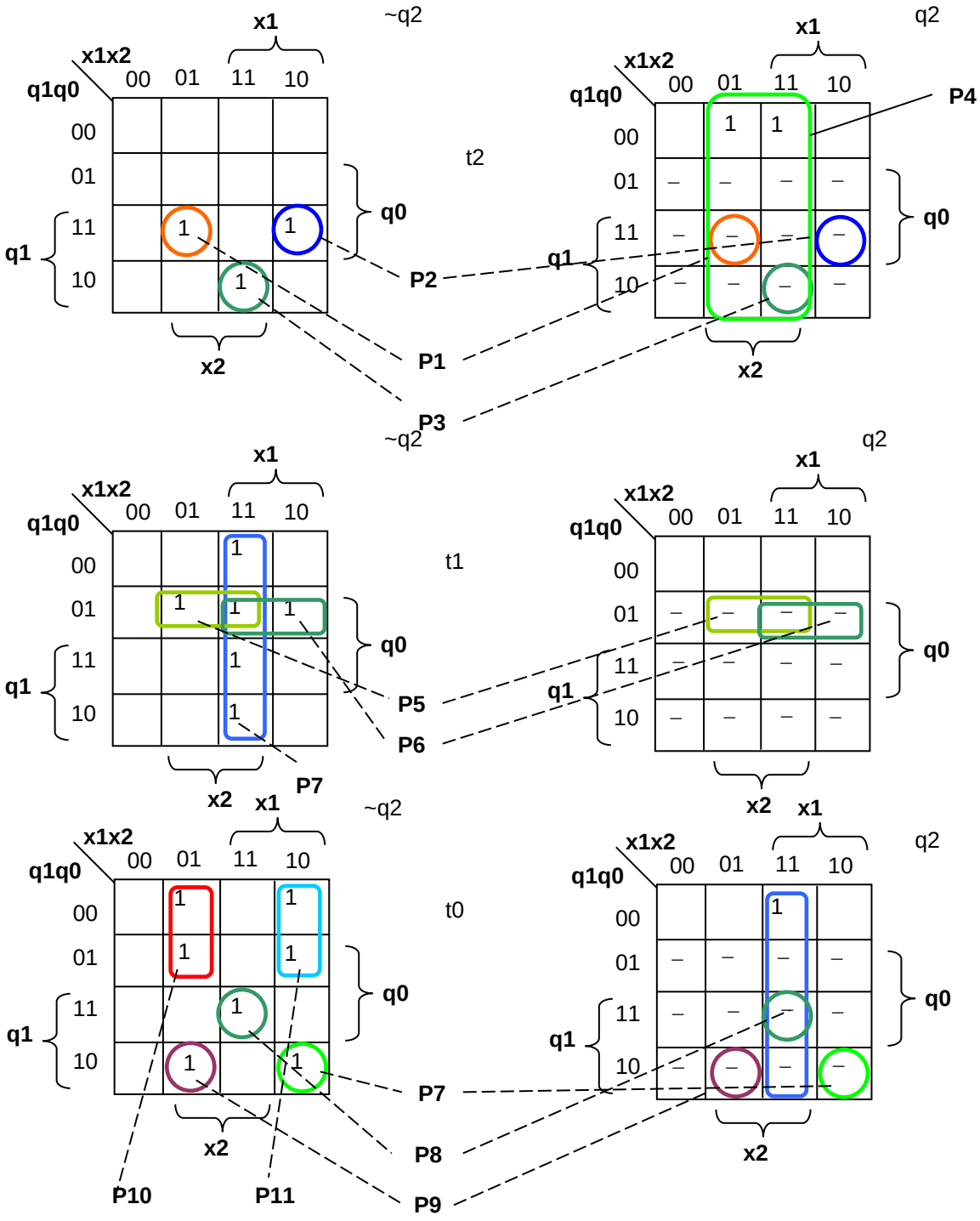




d2 = q1·q0·~x1·x2 + q1·~q0·x1·x2 + q2·x1·x2 + q1·q0·x1·~x2
d1= q1·~x1·~x2 + q0·~q1·x2 +q1·~q0·~x1 + ~q1·~q2·x1·x2 +q0·~q1·x1+q1~q0x1~x2
d0 =~q2·~q0·~x1·x2+~q2·~q0·x1·x2 +~q0·q2·x1·x2+~q1·~q2·q0·~x1·x2+
+~q2·~q1·q0·x1·x2

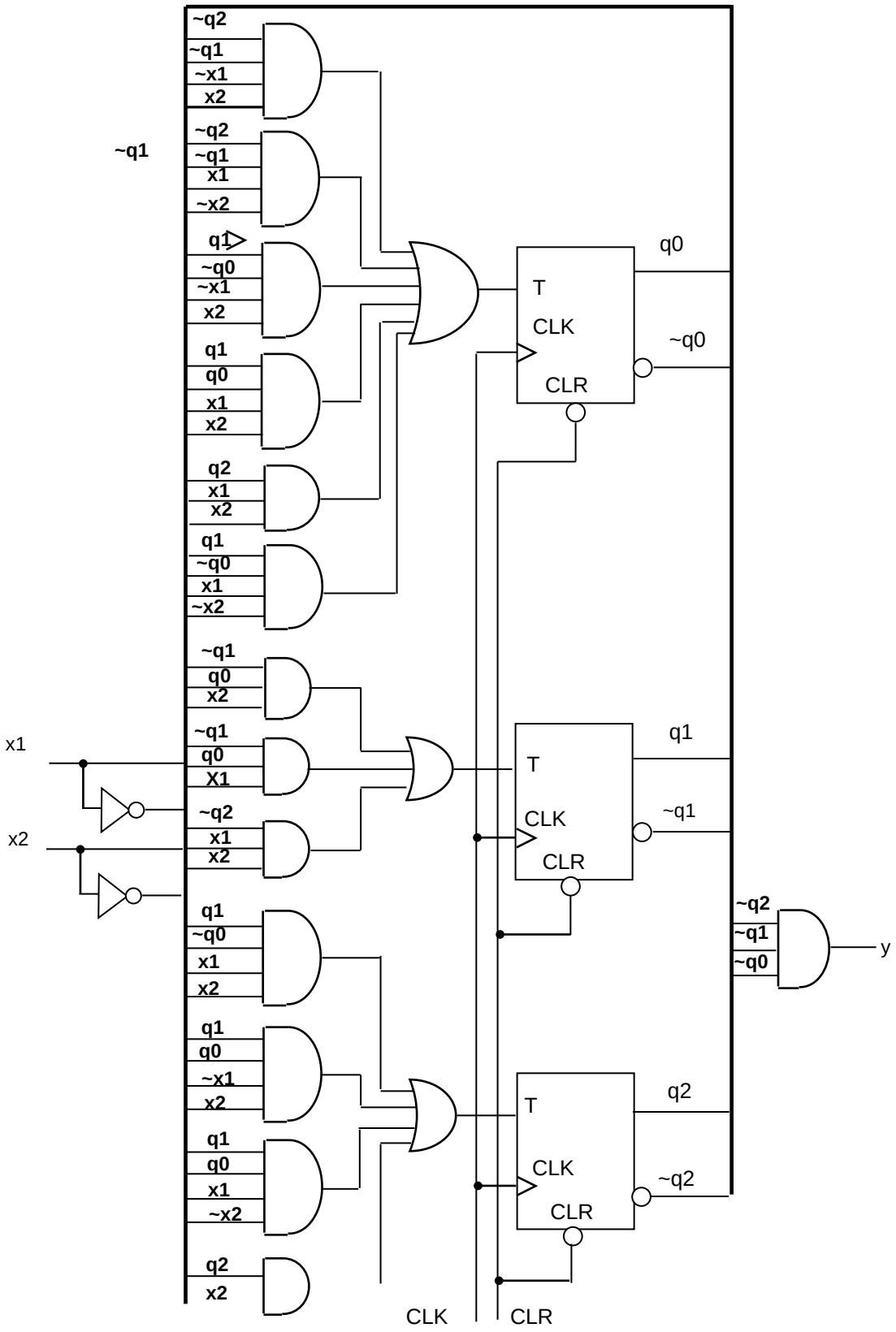
The number of gates' inputs is equal to 72.
The values of both examples are approximately the same.

Synthesis of FSM using T flip-flops
Excitation functions are shown in the table above.



t2=q1q0~x1x2 + q1~q0x1x2 + q1q0x1~x2 + q2x2;
t1=~q1q0x2 + ~q1q0x1 + ~q2x1x2
t0=~q2~q1~x1x2 + ~q2~q1x1~x2 + q2x1x2 + q1~q0~x1x2 + q1q0x1x2 + q1~q0x1~x2
The number of gates' inputs is equal to 63.
Definition of y=f(q2,q1,q0)
y= ~q2·~q1·~q0
The last variant of implementation should be chosen.

FSM circuit diagram



1b25.
The minimum signal formation time in some i-th net is defined by the following formula:

$$t_{bi}=\max[t_{b(i-1)} + t_{(i-1,\ i)}],$$

where t_{bi} ¨ $t_{b(i-1)}$– minimum limit times of i-th and (i-1)-th nets correspondingly; $t_{(i-1,\ i)}$- is the delay of the element for which (i-1)-th net is input and i-th net – output.
The maximum signal formation time in some i-th net is defined by the following formula:

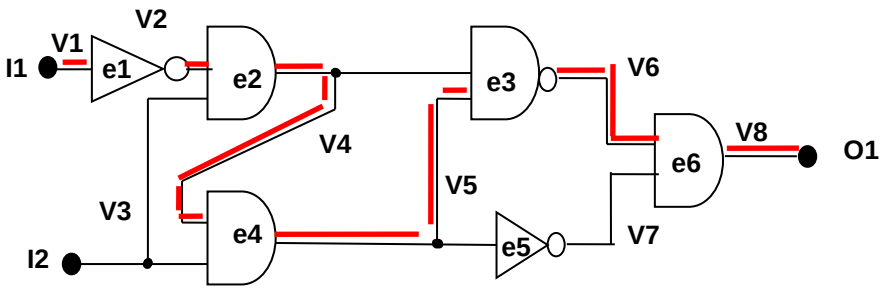
$$t_{ri}=\min[t_{r(i+1)} - t_{(i+1,\ i)}],$$

where t_{ri} ¨ $t_{r(i+1)}$– maximum limit times of i-th and (i+1)-th nets correspondingly; $t_{(i+1,\ i)}$- is the delay of the element for which (i+1)-th net is output and i-th net – input.
Time reserve for i-th net will be:

$$h_i = t_{maxi} - t_{mini}.$$

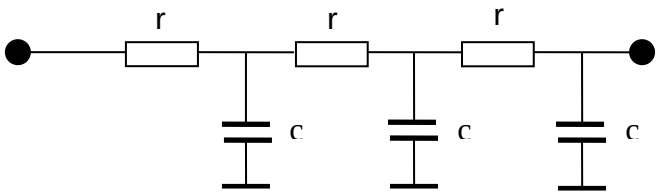
Calculation results are shown in the table

Net	V1	V2	V3	V4	V5	V6	V7	V8
t_{mini}	0	10	0	30	50	65	60	85
t_{maxi}	0	10	10	30	50	65	65	85



Critical path passes through all the nets for which $t_{bi}=t_{ri}$, i.e. V1, V2, V4, V5, V6, V8. The total delay of that path is 85.

1b26.
The equivalent circuit of interconnect's 3-segment, R,C distributed parameters will look like this:



The delay in it will be

$$\tau = rc + 2rc + 3rc = 6rc:$$

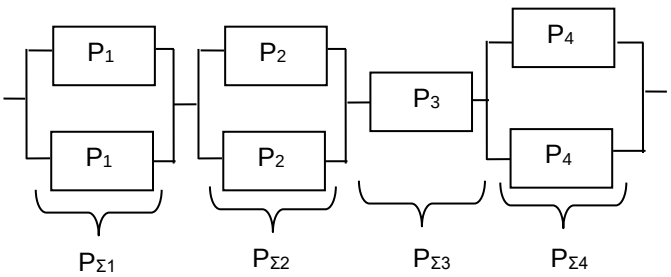
r =[(300:3):0,2]x0,1 = 50 Ohm,

$$c = \frac{300}{3}\cdot 0.1 = 10 \text{ fF}$$

c = (300:3)x0,1 = 10 fF,

$$\tau = 6x50x10 = 3000 \text{ OhmfF} = 3 \text{ ns}.$$

1b27.
Present the given circuit in the view of 4 sequentially connected regions:



Designate faultness probabilities of those regions

$$P_{\Sigma 1}, P_{\Sigma 2}, P_{\Sigma 3}, P_{\Sigma 4}.$$

Using probability summing, multiplication and full probability laws, the following can be written:

$$P_{\Sigma 1} = P_1P_1 + 2P_1(1-P_1)= P_1(2-P_1)=0,5(2-0,5)=0,75$$

$$P_{\Sigma 2} = P_2(2-P_2)=0,84$$

$$P_{\Sigma 3} = P_3=0,8$$

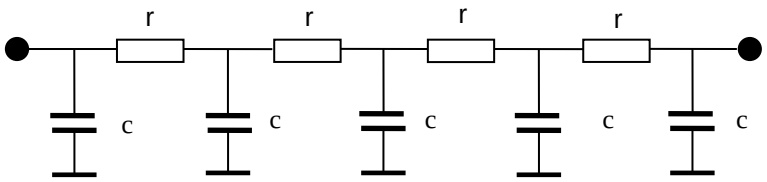
$$P_{\Sigma 4} = P_4(2-P_4)=0,64$$

The faultness probability of the circuit will be:

$$P= P_{\Sigma 1} \cdot P_{\Sigma 1} \cdot P_{\Sigma 1} \cdot P_{\Sigma 1}=0,75 \cdot 0,84 \cdot 0,8 \cdot 0,64=0,32256.$$

1b28.

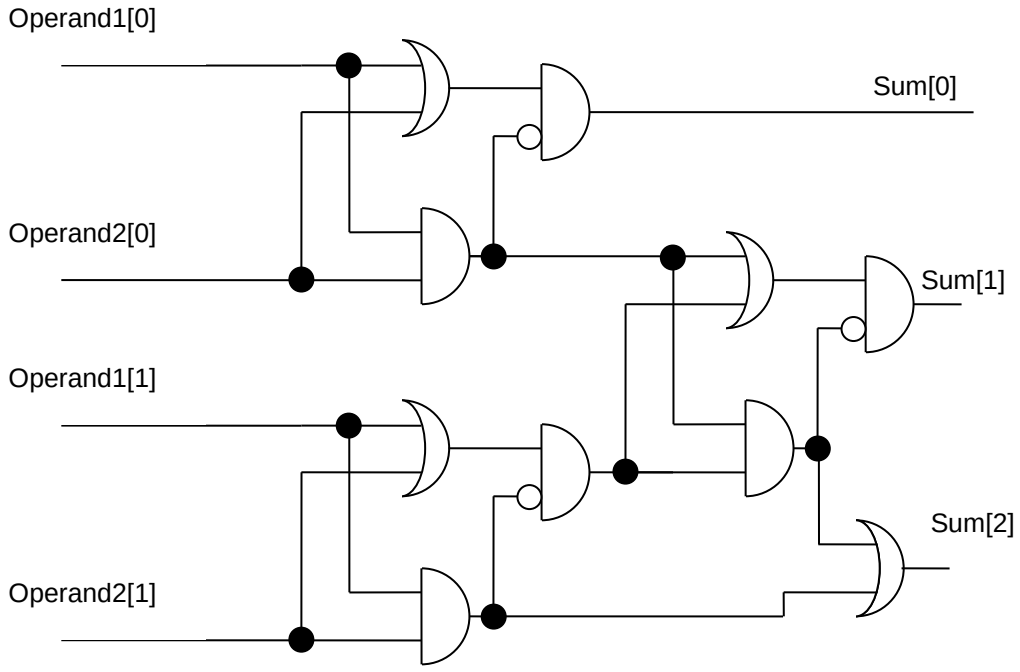
R, C equivalent circuit of interconnect will look as follows:



The delay in the transmission line connecting two contacts will be:

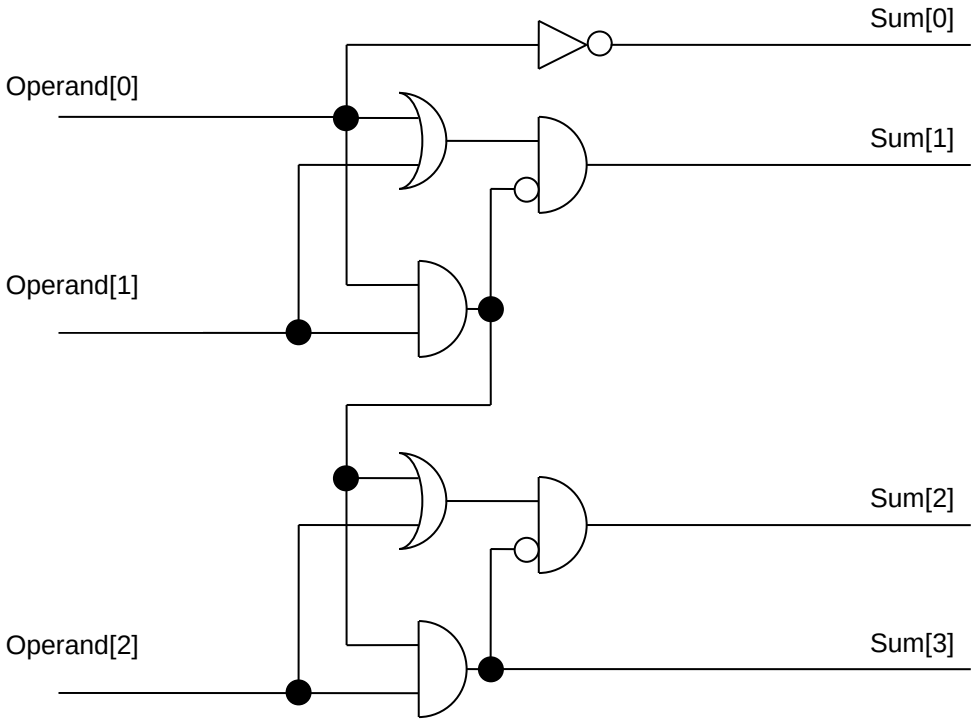
$$\tau = rc + 2rc + 3rc + 4rc = 10rc=10 \cdot 1 \cdot 100=1000 \text{ OhmfF} = 10 \text{ ns}.$$

1b29.



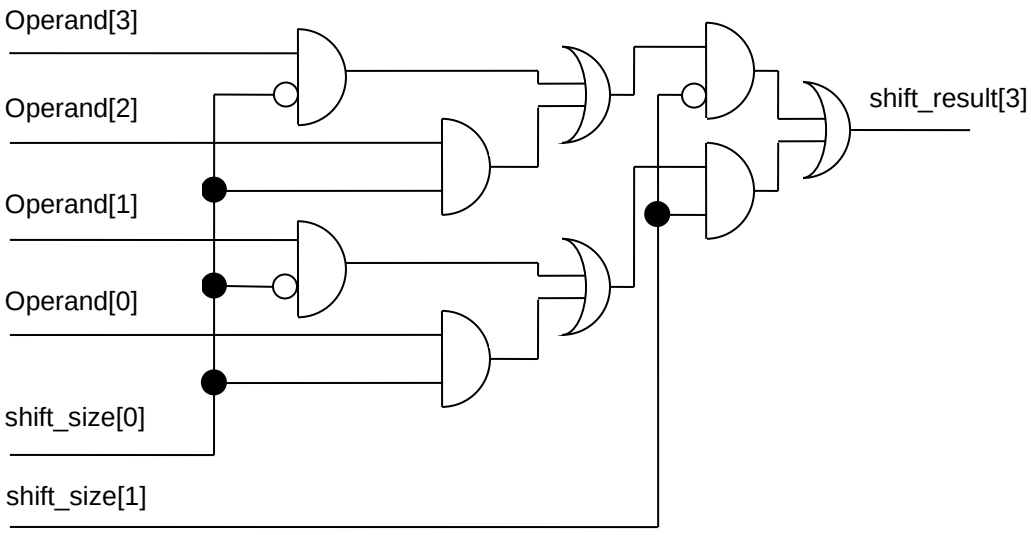
Yes, given logic is a pure combinatorial logic as it doesn't contain any memory elements and any logical feedbacks. Also, the outputs are only and only dependent from the inputs (from the combinations of inputs).

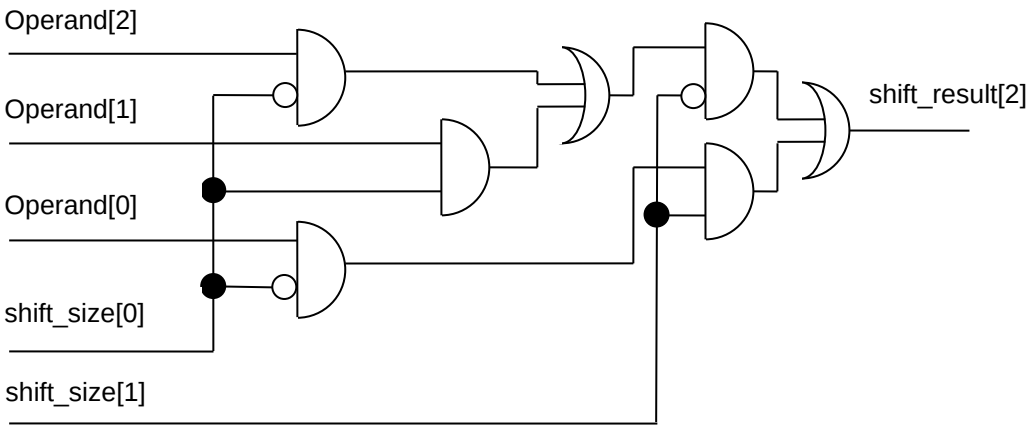
1b30.

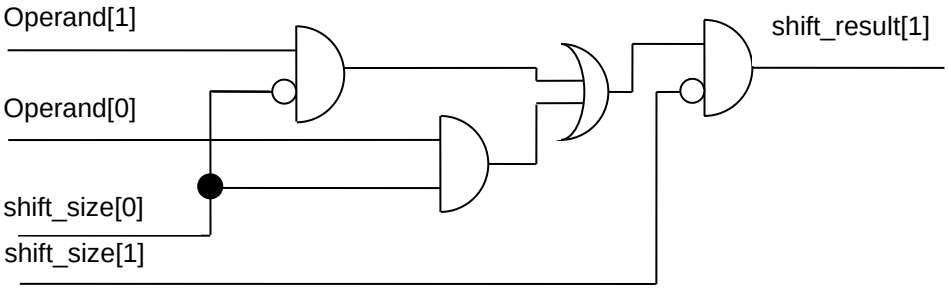


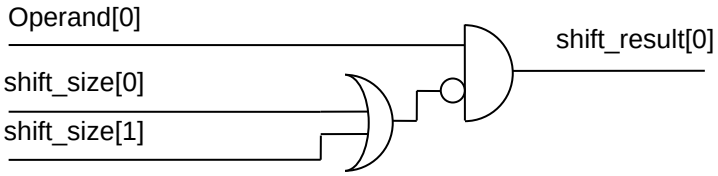
Yes, given logic is a pure combinatorial logic as it doesn't contain any memory elements and any logical feedbacks. Also, the outputs are only and only dependent from the inputs (from the combinations of inputs).

1b31.



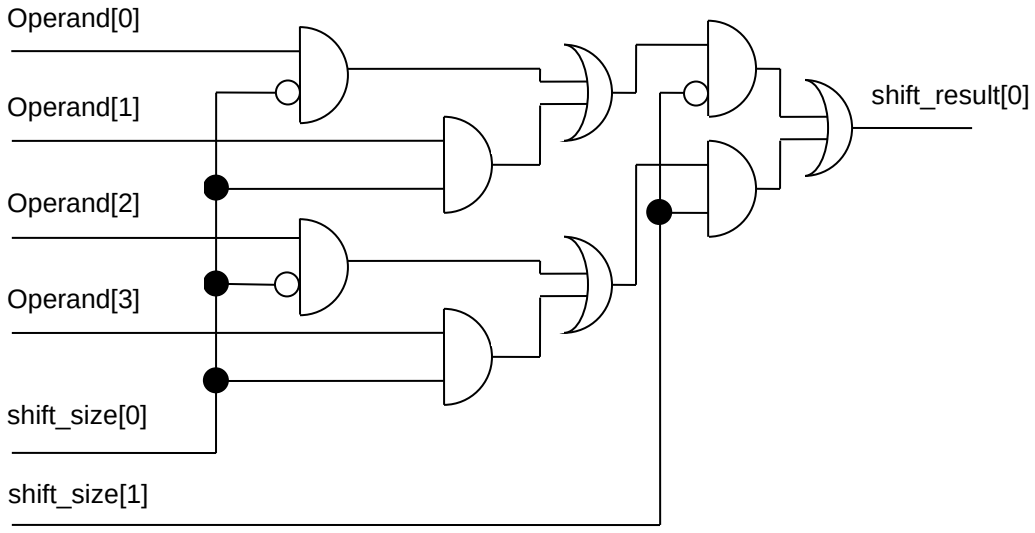


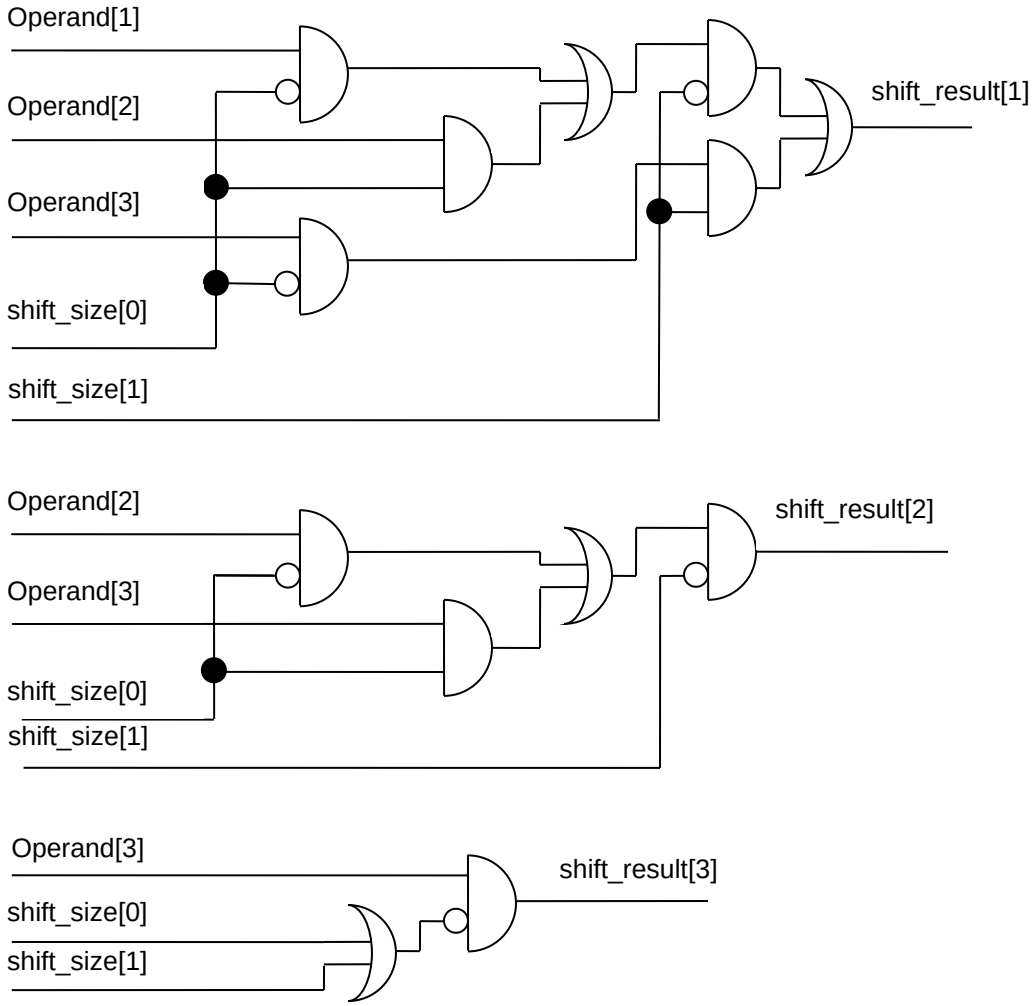




Yes, given logic is a pure combinatorial logic as it doesn't contain any memory elements and any logical feedbacks. Also, the outputs are only and only dependent from the inputs (from the combinations of inputs).

1b32.





Yes, given logic is a pure combinatorial logic as it does not contain any memory elements and any logical feedbacks. Also, the outputs are only and only dependent from the inputs (from the combinations of inputs).

1b33.

$t_{d1}=R_1C_{L1}=R_12yC_{in1}=2yR_1C_{in1}=2yR_1C$
$t_{d2}=R_2C_{L2}=(R_1/y)3z\ C_{in1}=3zR_1C/y$
$t_{d3}=R_3C_{L3}=(R_1/z)4.5C_{in1}=4.5R_1C/z$
$t_d=t_{d1}+t_{d2}+t_{d3}=R_1C(2y+3z/y+4.5/z)$
$\partial t_d/\partial z= R_1C(3/y-4.5/z^2)=0$
$\partial t_d/\partial y= R_1C(2-3z/y^2)=0$

From the solution of system y=1.275; z=1.084.

1b34.
Answer: 0.29 V

1b35.
When $V_{in}=V_H$, NMOS is in active mode, and PMOS is in saturated mode.

$$C_{ox}=\frac{\varepsilon_{ox}\varepsilon_0}{T_{ox}}=\frac{3.9\cdot 8.854\cdot 10^{-14}}{10^{-6}}=3.45\cdot 10^{-7}\,F/cm^2$$

$k_p=\mu_pC_{ox}= 241*10^{-7}A/V^2=24.1\mu A/V^2$; $k_n=\mu_nC_{ox}= 93.15\mu A/V^2$;

a.$V_{OH}=V_{DD}=1.8$ V,

$$\beta_p(VDD - V_{TP})^2 / 2 = \beta_n((VDD - V_{TN})V_{OL} - V_{OL}^2 / 2)$$

$$V_{OL} = (VDD - V_T)(1 - \sqrt{1 - \frac{\beta_p}{\beta_n}})$$

a. $\beta_p = k_p(W/L)p = 669.4\ \mu A/V2$
$\beta_n = k_n(W/L)n = 10350\ \mu A/V2$
$V_{OL}=(1.8-0.5)(1-(1-669.4/10350)^{0.5})=0.043$ V

$V_{OL}=0.043V$; $V_{OH}=VDD=1.8$ V,

b. $b_n = 4k_n(W/L)n = 41400\ \mu A/V2$
$V_{OL}=(1.8-0.5)(1-(1-669.4/41400)^{0.5})=0.011$ V

$V_{OL}=0.011V$; $V_{OH}=VDD=1.8$ ì

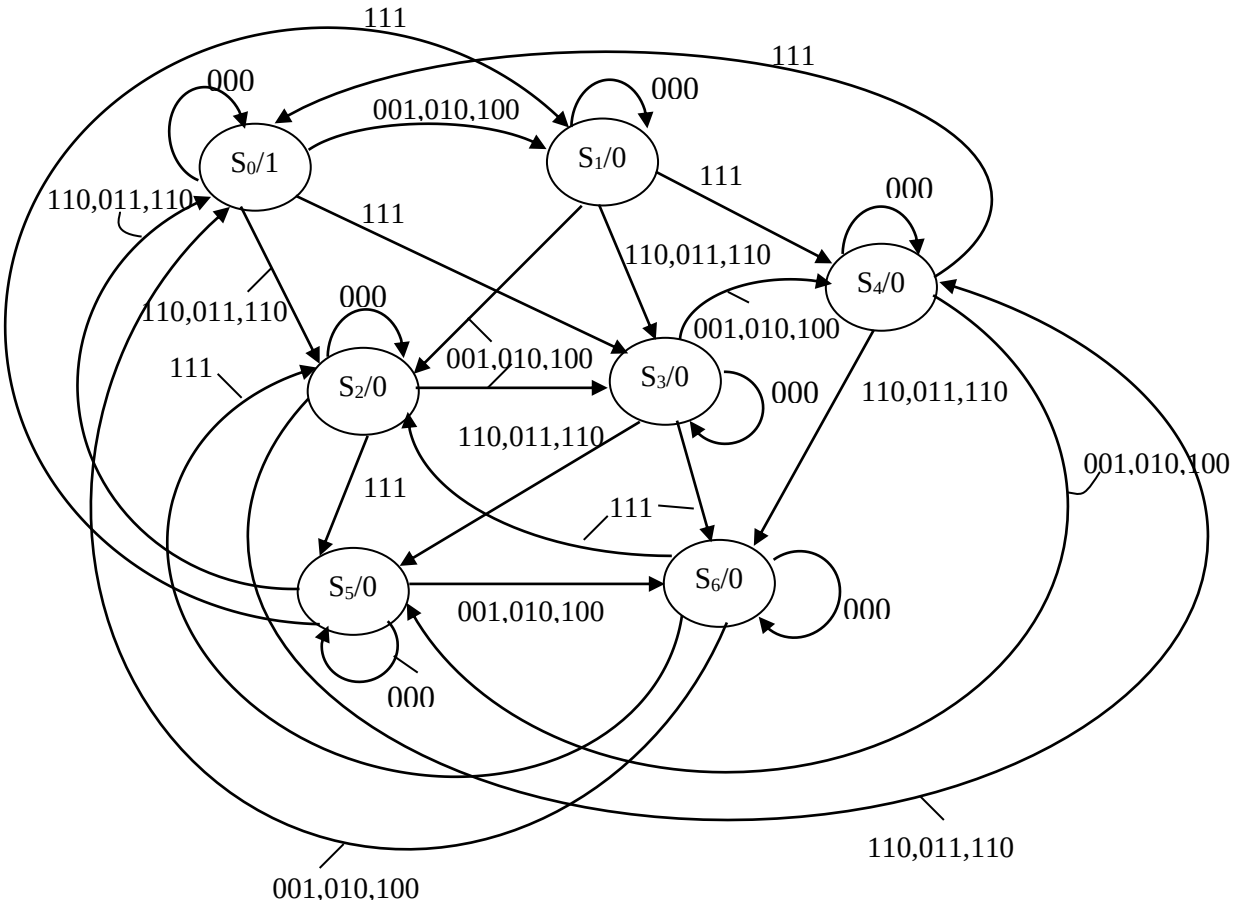
1b36.
Minimum range of clock pulses in digital circuits is defined from the condition of not violating setup time of flip-flop:
$T_{CLKmin} = t_{c2q}+t_{pinv}+t_{su} = 100+30+20=150ps$

1b37.

a. $\Delta V_V = \frac{C_{AV}}{C_V + C_{AV}} \Delta V_A = \frac{100}{60+100} \cdot 1 = 0.625V$

b. $C_{Vsw}=C_V+2C_{AV}=60+2Ē100=260$ fF

1b38.
Design of Moore's FSM:



Description of FSM by Verilog

```
module  fsm(in,out,clk,reset);
input  clk,reset;
input[2:0] in;
output  out;
reg  out;
reg[2:0]  state, next_state;
parameter  s0=3'b000, s1=3'b001, s2=3'b010, s3=3'b011,
s4=3'b100,s5=3'b101,s6=3'b110;
//state register
always @(posedge clk or negedge reset)
      begin
      if (!reset) state=s0;
            else state=next_state;
      end

//next state logic
always @(state or in)
      begin
            case (state)
            s0: case (in)
            3'b000:     ßnext_state=state;
            3'b001,3'b010,3'b100: next_state=s1;
            3'b011,3'b101,3'b110: next_state=s2;
            3'b111:           next_state=s3;
            default:          next_state=s0;
            endcase
s1: case (in)
      3'b000:           next_state=state;
      3'b001,3'b010,3'b100: next_state=s2;
      3'b011,3'b101,3'b110: next_state=s3;
      3'b111:           next_state=s4;
      default:          next_state=s0;
      endcase
 s2: case (in)
            3'b000:           next_state=state;
            3'b001,3'b010,3'b100: next_state=s3;
            3'b011,3'b101,3'b110: next_state=s4;
            3'b111:           next_state=s5;
            default:          next_state=s0;
            endcase
      s3: case (in)
      3'b000:           next_state=state;
      3'b001,3'b010,3'b100: next_state=s4;
      3'b011,3'b101,3'b110: next_state=s5;
      3'b111:           next_state=s6;
      default:          next_state=s0;
      endcase
            s4: case (in)
            3'b000:           next_state=state;
            3'b001,3'b010,3'b100: next_state=s5;
            3'b011,3'b101,3'b110: next_state=s6;
            3'b111:           next_state=s0;
            default:          next_state=s0;
            endcase
s5: case (in)
      3'b000:           next_state=state;
      3'b001,3'b010,3'b100: next_state=s6;
      3'b011,3'b101,3'b110: next_state=s0;
      3'b111:           next_state=s1;
      default:          next_state=s0;
```

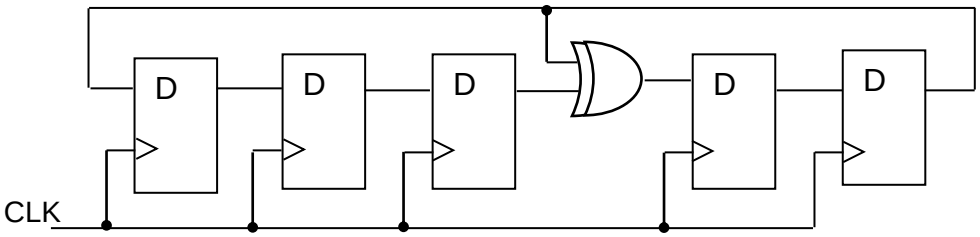
```
      endcase
            s6: case (in)
            3'b000:           next_state=state;
            3'b001,3'b010,3'b100: next_state=s0;
            3'b011,3'b101,3'b110: next_state=s1;
            3'b111:     next_state=s2;
            default:          next_state=s0;
            endcase
default: next_state=s0;
endcase
end
      //output logic
always @(state)
      if (state==s0)
      out=1'b1;
else out=1'b0;
endmodule
```

Testbench

```
module stimulus;
reg[2:0] in;
reg clk, reset;
fsm test(in,out,clk,reset);
initial begin
     clk=0;
     reset=1;
     #10 reset = 0;
     in=0;
     #13 reset = 1;
     #10 in = 3'd0;
     #10 in = 3'd2;
     #10 in = 3'd1;
     #10 in = 3'd3;
     #10 in = 3'd5;
     #10 in = 3'd0;
     #10 in = 3'd4;
     #10 in = 3'd7;
     #10 in = 3'd1;
     #10 in = 3'd7;
     #10 in= 3'd0;
     #10 $finish;
end
always #5 clk = ~clk;
endmodule
```

1b39.

The circuit of polynomial is presented in the figure.



The description of the counter by Verilog

```
module polynomial_counter (clk, preset, q);
input        clk, preset;
output[0:4] q;
reg [0:4]  q;
```

```
always       @(posedge clk or negedge preset)
      if    (!preset)
      q= 5'b10000;
      else q={q[4], q[0], q[1],q[2]^q[4], q[3]};
endmodule
```

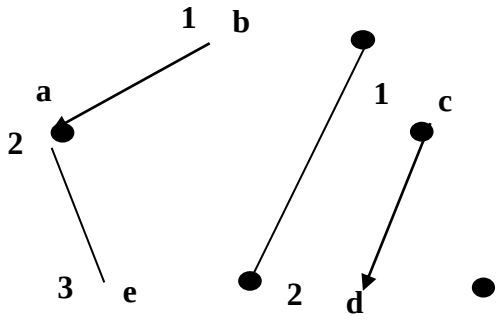
Testbench

```
module stimulus;
reg clk, preset;
wire[0:4] q;
polynomial_counter      test(clk,preset,q);
      initial begin
         clk=0;
         preset=1;
         #3 preset=0;
         #20 preset = 1;
         #200 $finish;
      end
always #5 clk=~clk;
endmodule
```

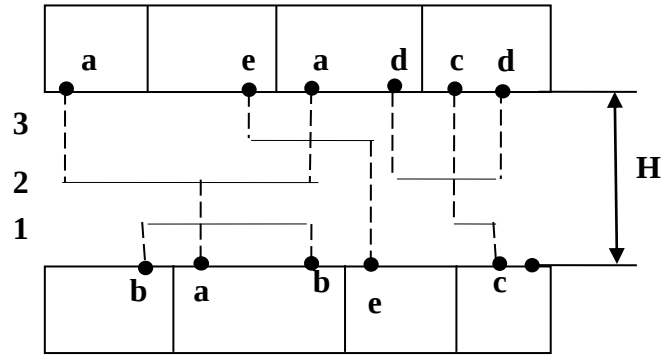
1b40.
The problem is solved in two phases:

- Definition of minimum number of horizontal channels;
- Calculation of minimum H distance between two rows of cells.

Construct horizontal and vertical limitations graph of a, b, c, d, e nets and heuristically define its chromatic number, as shown in the figure below.



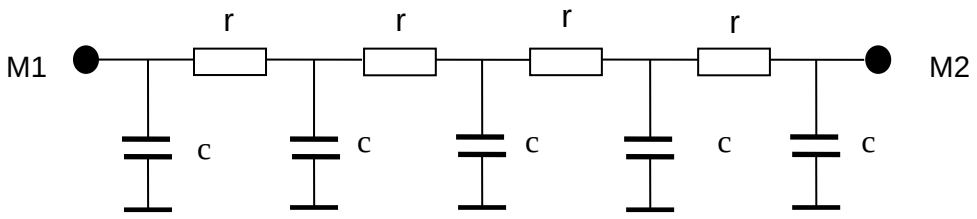
As seen from the figure, chromatic number of the graph equals 3. Hence it follows that for two-layer reciprocally perpendicular routing of the given nets, at least 3 horizontal channels are needed, as shown in the figure.



Thus, the minimum H distance between two rows of cells will be defined by the formula, shown below.
H= 3*0,1 + 2*0,1 + 2*0,2=0,9 um.

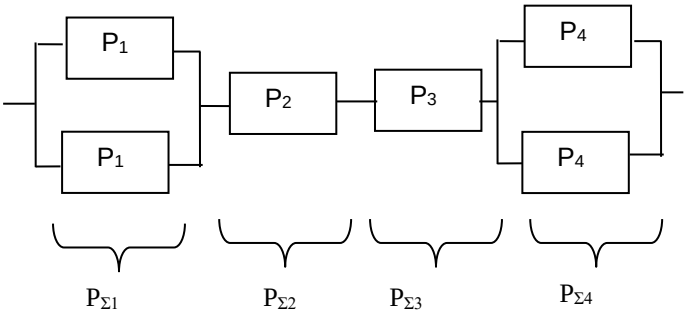
1b41.
The solution of the problem is based on the fact that N-MOS transistor is open, if “1” logic level signal is given to its gate, and P-MOS transistor - “0” logic level signal. Therefore the solution of the problem is the following:
a) T1, T2, T3, T4, T5, T6 →“0”;
b) T1, T3 →“0” ; T2, T4, T5, T6 →“1”.

1b42.
R, C equivalent circuit of M1-M2 transmission line will look as follows:



The delay in the transmission line, connecting two modules, will be:
$\tau = rc + 2rc + 3rc + 4rc = 10rc = 10x10x100 = 10000$ OhmfF = 10 ns.

1b43.
Present the given circuit in the form of 4 sequentially connected regions:



Designate the probabilities of faultless operation of those regions $P_{\Sigma 1}$, $P_{\Sigma 2}$, $P_{\Sigma 3}$, $P_{\Sigma 4}$.
Using the rules of addition, multiplication of probabilities and full probabilities, the following can be written:
$P_{\Sigma 1} = P_1P_1 + 2P_1(1-P_1) = P_1(2-P_1) = 0,5(2-0,5) = 0,75$
$P_{\Sigma 2} = P_2 = 0,6$
$P_{\Sigma 3} = P_3 = 0,8$
$P_{\Sigma 4} = P_4(2-P_4) = 0,64$
The probability of faultless operation of the circuit will be
$P = P_{\Sigma 1} \times P_{\Sigma 1} \times P_{\Sigma 1} \times P_{\Sigma 1} = 0,75x0,6x0,8x0,64 = 0,2304$.

2. ANALOG INTEGRATED CIRCUITS

a) Test questions

2a1. D
2a2. D
2a3. E
2a4. E
2a5. B
2a6. E
2a7. B
2a8. E
2a9. B
2a10. E
2a11. E
2a12. D
2a13. C
2a14. C
2a15. C
2a16. A
2a17. C
2a18. C
2a19. E
2a20. A
2a21. C
2a22. D
2a23. D
2a24. D
2a25. E
2a26. D
2a27. E
2a28. E
2a29. D
2a30. B
2a31. A
2a32. B
2a33. E
2a34. C
2a35. B
2a36. C
2a37. C
2a38. E
2a39. B
2a40. C
2a41. B
2a42. E
2a43. B
2a44. D
2a45. C
2a46. D
2a47. E
2a48. A
2a49. E
2a50. E
2a51. D
2a52. E
2a53. C
2a54. A
2a55. D
2a56. A
2a57. D

b) Problems

2b1.

$$I_{D2} = I_{ref}\left(\frac{W_2}{L_2}\right)\Big/\left(\frac{W_1}{L_1}\right) = I_{ref}$$

$$\left|I_{D3}\right| = \left|I_{D2}\right|,\ I_{D3} = I_{ref}$$

$$I_{D4} = I_{D3}\left(\frac{W_4}{L_4}\Big/\frac{W_3}{L_3}\right)$$

$$I_{D4} = I_{ref}$$

2b2.

$$\left(V_{in} - V_{TH1}\right)^2 \cdot W_1 \cdot \mu_n \cdot \frac{C_{ox}}{L_1} \cdot 2 = \left(V_{DD} - V_{TH1} - V_{out}\right)^2 \cdot W_2 \cdot \mu_n \cdot \frac{C_{ox}}{L_2} \cdot 2$$

$$\sqrt{\frac{W_1}{L_1}} \cdot \left(V_{in} - V_{TH1}\right) = \sqrt{\frac{W_2}{L_2}} \cdot \left(V_{DD} - V_{TH1} - V_{out}\right)$$

$$\sqrt{\frac{W_1}{L_1}} = \sqrt{\frac{W_2}{L_2}} \cdot \frac{dV_{out}}{dV_{in}}$$

$$K = \frac{dV_{out}}{dV_{in}} = -\sqrt{\frac{W_1 - L_2}{W_2 - L_1}}$$

2b3.

$$(V_{in}-V_{TH})^2\cdot W_1\cdot\mu_1\cdot\frac{C_{ox}}{L_1}\cdot 2=(VDD-V_{TH}-V_{out})^2\cdot W_2\cdot\mu_n\cdot\frac{C_{ox}}{L_2}\cdot 2$$

Saturation condition $V_{out}=V_{in}-V_{TH}$

$$(V_{in}-V_{TH})^2\cdot W_1\cdot\mu_n\cdot\frac{C_{ox}}{L_1}\cdot 2=(V_{DD}-V_{TH}-(V_{in}-V_{TH}))^2\cdot W_2\cdot\mu_n\cdot\frac{C_{ox}}{L_2}\cdot 2$$

$$7\cdot(V_{in}-V_{TH})=3\cdot(V_{DD}-V_{TH})$$

$$10\cdot V_{in}=13.9$$

$$V_{in}=1.39\,\text{V}$$

2b4.

$$I=\frac{V_{g2}+2.5V}{R}=\frac{\beta}{2}\cdot(V_{g2}-V_{g1}-V_{TH2})^2=\frac{\beta}{2}\cdot(V_{g1}-2.5-V_{TH1})^2$$

$$V_{g2}-V_{g1}-V_{TH2}=V_{g1}-2.5-V_{TH1}$$

$$V_{g1}=\frac{V_{g2}-2.5}{2}$$

$$I=\frac{2\cdot V_{g1}}{R}=\frac{\beta}{2}\cdot(V_{g1}-2.5-V_{TH1})^2$$

2b5.

$I_{D2}=I_{ref}((W_2/L_2)/(W_1/L_1))$

$|I_{D3}|=|I_{D2}|$

$I_{D4}=I_{D3}((W_4/L_4)/(W_3/L_3))$

$I_{D4}=I_{ref}((W_2/L_2)/(W_1/L_1))((W_4/L_4)/(W_3/L_3))$

$I_{D4}=I_{ref}((W_2L_1)/(W_1L_2))((W_4L_3)/(W_3L_4))$

$$I_{D4}=I_{ref}\frac{W_2W_4L_1L_3}{W_1W_3L_2L_4}$$

2b6.

$$R=\frac{V_{DD}-V_{ref}}{I}$$

$$I=\frac{\beta}{2}(V_{GS}-V_{THN})^2=\frac{\beta}{2}(V_{ref}-V_{THN})^2$$

$$\beta=K_n\frac{W}{L}=\mu_n\frac{\varepsilon_{Si}\cdot\varepsilon_0}{t_{ox}}\cdot\frac{W}{L}=120\ \text{uA/V}^2$$

$$I=0.6\cdot10^{-4}(V_{ref}-0.8)^2$$

$$V_{ref} = V_{DD} - IR$$
$$V_{ref} = 2 - 10^4 \cdot 10^{-4} \cdot 0.6(V_{ref} - 0.8)^2$$
$$V_{ref} = 2 - 0.6(V^2{}_{ref} - 1.6V_{ref} + 0.64)$$
$$V_{ref} = 2 - 0.6V^2{}_{ref} + 0.96V_{ref} - 0.384$$
$$-0.6V^2{}_{ref} - 0.04V_{ref} + 1.616 = 0$$
$$0.6V^2{}_{ref} + 0.04V_{ref} - 1.616 = 0$$
$$V_{ref1,2} = \frac{-0.04 \pm \sqrt{0.0016 + 3.8784}}{1.2}$$
$$V_{ref1,2} = \frac{-0.04 \pm 1.97}{1.2}$$
$$V_{ref} = \frac{-0.04 + 1.97}{1.2} = 1.675 \text{ V}$$

2b7.

a) When V_{DD} increases by 10%.

$$I_{out} = \frac{\beta}{2}(V_A - V_{TH})^2$$
$$V_A = \frac{R_2}{R_1 + R_2} V_{DD}$$
$$\Delta I_{out} = \frac{\beta}{2}[(\frac{R_2}{R_1 + R_2} V_{DD} - V_{TH})^2 - (\frac{R_2}{R_1 + R_2} 1.1V_{DD} - V_{TH})^2]$$
$$\beta = K_n \frac{W}{L} = 120 \cdot 10^{-6} \cdot \frac{50}{0.5} = 12 \quad \text{uA/V}^2$$
$$\Delta I_{out} = 6 \cdot 10^{-3}\left[(0.78 - 0.5)^2 - (0.858 - 0.5)^2\right] = 6 \cdot 10^{-3}(0.0784 - 0.128) \approx -0.3$$
$$\Delta I_{out} = -0.3 \text{ mA (increases by 0.3 mA)}$$

b) When V_{DD} reduces by 10%.

$$\Delta I_{out} = \frac{\beta}{2}[(\frac{R_2}{R_1 + R_2} V_{DD} - V_{TH})^2 - (\frac{R_2}{R_1 + R_2} 0.9V_{DD} - V_{TH})^2]$$
$$\Delta I_{out} = 6 \cdot 10^{-3}(0.0784 - 0.0408) \approx 0.23$$
$$\Delta I_{out} = 0.23 \text{ mA} \quad \text{(reduces by 0.23 mA)}$$

2b8.

$$K = -\frac{R_2 \,||\, X_C}{R_1}$$
$$K = -\frac{R_2 \cdot \frac{1}{j\omega C}}{R_1(R_2 + \frac{1}{j\omega C})}$$

$$K = -\frac{R_2}{R_1(\,j\omega R_2 C + 1)} = -\frac{R_2}{R_1}\cdot\frac{1 - j\omega R_2 C}{1+\omega^2 {R_2}^2 C^2}$$

$$|K| = \frac{R_2}{R_1}\cdot\frac{1}{\sqrt{1+\omega^2 {R_2}^2 C^2}}$$

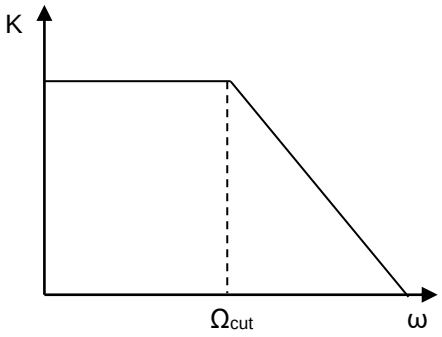
$\omega=0 \Rightarrow$ $K = -\frac{R_2}{R_1}$, $\frac{\frac{R_2}{R_1}\cdot\frac{1}{\sqrt{1+\omega^2 {R_2}^2 C^2}}}{\frac{R_2}{R_1}} = \sqrt{2}$

$$\frac{1}{\sqrt{1+\omega^2 {R_2}^2 C^2}} = \frac{1}{\sqrt{2}}$$

$$1+\omega^2 {R_2}^2 C^2 = 2$$

$$\omega^2 {R_2}^2 C^2 = 1 \qquad \omega_{cut} = \frac{1}{R_2 C}$$

$$\omega >> \frac{1}{R_2 C} \Rightarrow K \to 0$$



2b9.

$$I_D = I_{OUT} = (V_{GS} - V_{TH})\frac{g_m}{2} \quad (1)$$

$$V_{GS} = V_G = \frac{R_2}{R_1 + R_2}\cdot VDD \quad (2)$$

Putting (2) in (1), the following will be obtained:

$$I_{OUT} = (\frac{R_2}{R_1 + R_2}\cdot VDD - V_{TH})\cdot\frac{g_m}{2}$$

2b10.

$$V_{OUT} = VDD - R_D(I_D + \frac{V_{OUT} - V_{in}}{R_F})$$

$$V_{OUT} = \frac{VDD - R_D I_D - \frac{R_D}{R_F} V_{in}}{1 + \frac{R_D}{R_F}}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$V_{GS} = V_b - V_{in}$$

$$V_{OUT} = \frac{VDD - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_B - V_{in} - V_{TH})^2 - \frac{R_D}{R_F} V_{in}}{1 + \frac{R_D}{R_F}}$$

2b11.

$$V_- = -\frac{V_{out}}{K_A}$$

$$I_4 = I_1 + I_2 + I_3$$

$$\frac{V_- - V_{out}}{R_4} = \frac{V_{in1} - V_-}{R_1} + \frac{V_{in2} - V_-}{R_2} + \frac{V_{in3} - V_-}{R_3}$$

$$\frac{-\frac{V_{out}}{K_A} + V_{out}}{R_4} = \frac{V_{in1} + \frac{V_{out}}{K_A}}{R_1} + \frac{V_{in2} + \frac{V_{out}}{K_A}}{R_2} + \frac{V_{in3} + \frac{V_{out}}{K_A}}{R_3}$$

$$-V_{out}(1 + \frac{1}{K_A}) \cdot R_1 R_2 R_3 = V_{in1} \cdot R_4 R_2 R_3 + V_{out} \frac{1}{K_A} \cdot R_4 R_2 R_3 + V_{in2} R_4 R_1 R_3 +$$

$$+ V_{out} \cdot \frac{1}{K_A} \cdot R_4 R_1 R_3 + V_{in3} \cdot R_4 R_1 R_2 + V_{out} \frac{1}{K_A} R_4 R_1 R_2$$

$$V_{out}(\frac{1}{K_A} R_4 (R_2 R_3 + R_1 R_3 + R_1 R_2) + (1 + \frac{1}{K_A}) \cdot R_1 R_2 R_3) = -R_4 (V_{in1} R_2 R_3 + V_{in2} R_1 R_3 + V_{in3} R_1 R_2)$$

$$V_{out} = -\frac{R_4 (V_{in1} R_2 R_3 + V_{in2} R_1 R_3 + V_{in3} R_1 R_2)}{\frac{1}{K_A} R_4 (R_2 R_3 + R_1 R_3 + R_1 R_2) + (1 + \frac{1}{K_A}) \cdot R_1 R_2 R_3}$$

2b12.

$$I_{m1} = I_{ref}$$

$$I_{m2} = 5 \cdot I_{m1} = 5 \cdot I_{ref}$$

$$I_{m3} = I_{m2} = 5 I_{ref}$$

$$I_{m4} = 5 I_{m3} = 25 I_{ref}$$

$$V_{out} = R_1 \cdot I_{m4} = 25 I_{ref} R_1$$

2b13.

$$|I_{D1}| = |I_{ref}|, \qquad I_{D2} = I_{D1} \left(\frac{W_2}{L_2}\right) \Big/ \left(\frac{W_1}{L_1}\right) = I_{ref}$$

$$|I_{D3}| = |I_{D2}|, I_{D3} = I_{ref}$$

$$I_{D4} = I_{D3} \left(\frac{W_4}{L_4}\right) \Big/ \left(\frac{W_3}{L_3}\right) = 0.5 I_{ref}$$

2b14.

$$I_{out} = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_A - V_{TH})^2, \qquad V_A = \frac{V_{DD}}{R_1 + R_2}R_2$$

$$\Delta I_{out} = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}\left[\left(\frac{V_{DD}}{R_1 + R_2}R_2 - V_{TH}\right)^2 - \left(\frac{1.1V_{DD}}{R_1 + R_2}R_2 - V_{TH}\right)^2\right]$$

$$\Delta I_{out} = -\frac{1}{2}\mu_n c_{ox}\frac{W}{L}\left(0.21\left(\frac{V_{DD}}{R_1 + R_2}R_2\right)^2 - 0.2\frac{V_{DD}}{R_1 + R_2}R_2 V_{TH}\right)$$

2b15.

$$R = \frac{V_{DD} - V_{ref}}{I}$$

$$I = I_1 + I_2 = \frac{V_{ref}}{R_1 + R_2} + \frac{\beta}{2}\left(\frac{V_{ref}}{R_1 + R_2}R_2 - V_{TH}\right)^2$$

$$R = \frac{V_{DD} - V_{ref}}{\frac{V_{ref}}{R_1 + R_2} + \frac{\beta}{2}\left(\frac{V_{ref}}{R_1 + R_2}R_2 - V_{TH}\right)^2}$$

2b16.

Relative to variable component

$$I_D = g_m V_{gs}$$

$$V_{out} = I_{D3} * R_1$$

$$\frac{I_{D3}}{g_{m3}} = \frac{I_{D2}}{g_{m2}}, \qquad I_{D2} = I_{D1} = g_{m1}V_{in}$$

$$V_{out} = \frac{g_{m1}g_{m3}R_1}{g_{m2}}V_{in}$$

$$k = \frac{dV_{out}}{dV_{in}} = \frac{g_{m1}g_{m3}R_1}{g_{m2}}$$

3. RF CIRCUITS

a) Test questions

3a1. A
3a2. A
3a3. B

4. SEMICONDUCTOR PHYSICS AND ELECTRONIC DEVICES

a) Test questions

4a1. D
4a2. A
4a3. B
4a4. C
4a5. B
4a6. B
4a7. C
4a8. C
4a9. A
4a10. B
4a11. A
4a12. C
4a13. B
4a14. D
4a15. E
4a16. A
4a17. C
4a18. C
4a19. C
4a20. B
4a21. E
4a22. C
4a23. C
4a24. C
4a25. E
4a26. C
4a27. B
4a28. C
4a29. C
4a30. A
4a31. D
4a32. E
4a33. C
4a34. C
4a35. B
4a36. C
4a37. C
4a38. C
4a39. B
4a40. D
4a41. D
4a42. D
4a43. B
4a44. B
4a45. B
4a46. B
4a47. C
4a48. A
4a49. D
4a50. B
4a51. A
4a52. B
4a53. C
4a54. C
4a55. B
4a56. B
4a57. B

b) Problems

4b1.

Diode's current-voltage characteristic:

$$J = J_s(e^{\frac{eV}{kT}} - 1)$$

Can be introduced by the following way:

$$\frac{dJ}{dV} = J_s \frac{e}{kT} exp\left(\frac{eV}{kT}\right) = \frac{e}{kT}(J_s + J),$$

from which for diode's differential resistance this will be obtained:

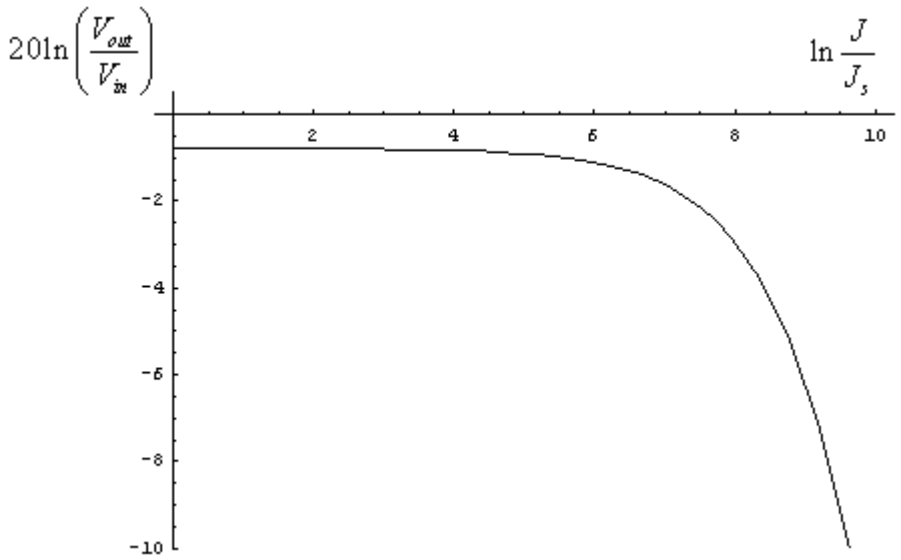
$$r = \frac{dV}{dJ} = \frac{kT}{e(J_s + J)} \ .$$

In the shown circuit, for signal decay there is:

$$\frac{V_{out}}{V_{in}} = \frac{r}{r+R} = \frac{\frac{kT}{e(J+J_s)}}{\frac{kT}{e(J+J_s)} + R}$$

The final view of decay expressed by decibels:

$$20\,ln\frac{V_{out}}{V_{in}} = 20\ ln\frac{\frac{kT}{e(J+J_s)}}{\frac{kT}{e(J+J_s)} + R}:$$



The obtained dependence of for the given parameters is shown in the figure.

4b2.

It is enough to be limited by the approximation of full depletion layer, according to which formation of a $p-n$ junction results in a depleted region at the p-n interface where the density of volume charge region is given by $\rho = -ekx$ expression. To find potential distribution, it is necessary to solve Poison equation in volume charge's $(-w,0)$ and $(0,w)$ regions:

$$\frac{d^2\varphi}{dx^2} = \frac{\rho}{\varepsilon\varepsilon_0} = -\frac{ekx}{\varepsilon\varepsilon_0}:$$

The general solution of this equation will be:

$$\varphi(x) = -\frac{ekx^3}{6\varepsilon\varepsilon_0} + C_1 x + C_2,$$

where the appeared unknown constants should be found from angle conditions requiring that $\varphi(0) = 0$ (start of potential calculation) and $\frac{d\varphi}{dx}(\pm w) = 0$. In the result the following will be formed:

$$\varphi(x) = -\frac{ekx^3}{6\varepsilon\varepsilon_0} + \frac{ekw^2}{2\varepsilon\varepsilon_0}x$$

Considering that $\varphi(w) - \varphi(-w) = \psi - V$ the following will be got:

$$w = \sqrt[3]{\frac{\varepsilon\varepsilon_0(\psi - V)}{ek}}:$$

The value of volume charge:

$$Q = A\int_0^w ekx\,dx = A\frac{ekw^2}{2} = A\frac{ek}{2}\left(\frac{\varepsilon\varepsilon_0(\psi - V)}{ek}\right)^{2/3},$$

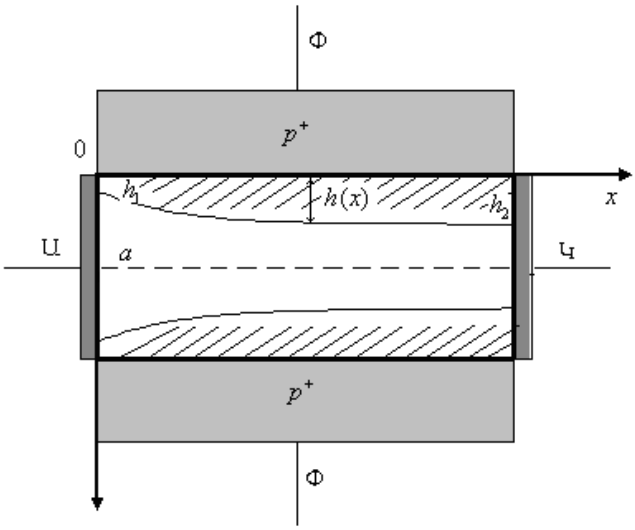
from which for junction capacitance the following will be formed:

$$C = \left|\frac{dQ}{dV}\right| = A\left(\frac{\varepsilon\varepsilon_0 ek}{12(\psi - V)}\right)^{1/3}:$$

Putting the data, the following will be written:

$$C \approx 46.5\,\text{pf}.$$

4b3.



The structure of the transistor is shown in the figure. It is convenient to insert the following function describing the integral density of the charge:

$$Q(y)=\int_0^y \rho(y)dy\ ,\ 0\le y\le h(x)\ , \tag{1}$$

where by the approximation of full depletion layer $\rho(y)=eN_D(y)$, and $h(x)$ is the width of depletion layer in $x=const$ plane. Reverse to V voltage, applied on p^+-n junction, it is necessary to use Poison equation in order to find the dependence of $h(x)$-and $\rho(y)$. Integrating it by y and considering that in $y=h(x)$ point the component of field intensity should be zero, the following will come out:

$$-\varepsilon_y=\frac{\partial\varphi}{\partial y}=\frac{1}{\varepsilon\varepsilon_0}[Q(h)-Q(y)] \tag{2}$$

This equation can be once more integrated according to y -0 to $h(x)$ considering that the change of potential should be equal to V .

$$V=\frac{1}{\varepsilon\varepsilon_0}\left[Q(h)\int_0^h dy-\int_0^h Q(y)dy\right]=\frac{1}{\varepsilon\varepsilon_0}\left[hQ(h)-\int_0^h Q(y)dy\right]=\frac{1}{\varepsilon\varepsilon_0}\int_0^h y\rho(y)dy \tag{3}$$

From here the following will be obtained:

$$\frac{dV}{dh}=\frac{h\rho(h)}{\varepsilon\varepsilon_0} \tag{4}$$

Now it is possible to go into transistor's calculation of current-voltage characteristic and transconductance. In every cross section of the channel x = const current value is constant and equals:

$$I_D=-eZ\mu_n\frac{dV}{dx}\int_{2a-h}^h N_D(y)dy=eZ\mu_n\frac{dV}{dx}2\int_h^a N_D(y)dy\ , \tag{5}$$

where $\varepsilon_x=-\frac{dV}{dx}$ is the component of field intensity, and channel width equals $2(a-h)$. From the last equation, the following is formed:

$$I_D dx=2eZ\mu_n dV\int_h^a N_D(y)dy=2eZ\mu_n\frac{dV}{dh}dh\int_h^a N_D(y)dy\ , \tag{6}$$

In this equation it has been considered that according to x (along the channel) change of potential takes place and if there is integration in the left part according to x from x=0 (start of the channel) to x=L (end of the channel),then on the right part it equals the change of potential from 0 to drain's V_D voltage. It is convenient to pass to according to h integration from according to potential integration, considering (4). In the result:

$$I_D = \frac{2Z\mu_n}{\varepsilon\varepsilon_0 L}\int_{h_1}^{h_2}[Q(a)-Q(h)]h\rho(h)dh\ , \tag{7}$$

Here h_1 and h_2 represent the edges of volume charge layer in x=0 and x=L cross sections (accordingly near the source and drain). According to definition, the transconductance will be:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\partial I_D}{\partial h_1}\frac{\partial h_1}{\partial V_G} + \frac{\partial I_D}{\partial h_2}\frac{\partial h_2}{\partial V_G} \tag{8}$$

where V_G is gate's (p^+- domain) voltage. Using (7) and (4) eventually the following is obtained:

$$g_m = \frac{2Z\mu_n}{L}[Q(h_2)-Q(h_1)]. \tag{9}$$

4b4.
R_h=3.33*10^{-4} m^3/Cl,
ρ=8.93*10^{-3} Ohm*m,
β=0.5 Ml,
φ=?
φ=μ*β, where μ is particle's mobility

$$\mu = \frac{R_h}{\rho} = \frac{3.33*10^{-4}}{8.93*10^{-3}}\ \text{m}^2/(\text{V*v}) = 3.73*10^{-2}\ \text{m}^2(\text{V*v})$$

φ=3.73*10^{-2}*0.5=1.86*10^{-2} rad.

4b5.
K_f=100 uA/lm,
Φ=0.15 lm
R=400 kOhm,
I=10 mA,
U=220 V,
Ku=?, Kp=?
Photovoltaic cell current:

$$I_f = K_f * \Phi = 15\ uA$$

Amplifier's input power:

$$\rho_m = I^2R = (15*10^{-6})^2*4*10^5 = 9*10^{-5}\ Vt$$

Power of relay:

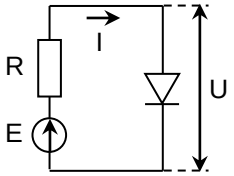
$$\rho_n = U*I = 220*10*10^{-3} = 2.2\ Vt$$

$$K_p = \frac{\rho_n}{\rho_\delta} = \frac{2.2}{9*10^{-5}} = 2.44*10^4$$

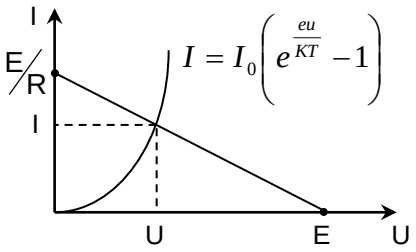
$$K_u = \frac{U_n}{U_R} = \frac{U_p}{I_f * R} = \frac{220}{10*10^{-6}*400*10^3} = 36.7$$

4b6.
I_0=8 uA,
E=10 V
R=1 kOhm,
T=300 K,
I=?, U=?
1.

$$I = I_0\left(e^{\frac{u}{\varphi_T}} - 1\right) = I_0\left(e^{\frac{E-IR}{(KT)/e}} - 1\right)$$



2.



4b7.

I_{hmax}=2 mA,
U_{gcut}=5 V
U_{g1}=-5 V
U_{g2}=0 V
U_{g3}=-2.5 V
I_h=?, S=?

1. $I_h = I_{hmax}\left(1 - \frac{|U_g|}{U_{gcut}}\right)^2$

$$I_{h1} = 2\left(1 - \frac{|-5|}{5}\right)^2 = 0$$

$$I_{h2} = 2\left(1 - \frac{|0|}{5}\right)^2 = 2$$

$$I_{h3} = 2\left(1 - \frac{|-2.5|}{5}\right)^2 = 0.5$$

2. $S = \frac{2 \cdot I_{hmax}}{U_{gcut}}\left(1 - \frac{|U_g|}{U_{gcut}}\right)^2$

$$S_1 = \frac{2 \cdot 2}{5}\left(1 - \frac{|-5|}{5}\right)^2 = 0$$

$$S_2 = \frac{2 \cdot 2}{5}\left(1 - \frac{|0|}{5}\right)^2 = 0.8$$

$$S_3 = \frac{2 \cdot 2}{5}\left(1 - \frac{|-2.5|}{5}\right)^2 = 0.2$$

4b8.

a. By the above mentioned values calculate the densities of majority carriers in *p*- and *n*- domains:

$$n_n = N_d = \frac{\sigma_n}{q\mu_n} = \frac{10}{1.6*10^{-19}*1300} = 4.8*10^{16}\,\text{cm}^{-3},$$

$$P_p = N_a = \frac{\sigma_p}{q\mu_p} = \frac{5}{1.6*10^{-19}*500} = 6.2*10^{16}\,\text{cm}^{-3}$$

When the external voltage is missing, the contact φ_k difference of potentials can be calculated by the following impression:

$$\varphi_k = \frac{kT}{q}\ln\frac{n_n p_p}{n_i^2} = \frac{1.38*10^{-23}300}{1.6*10^{-19}}\ln\frac{4.8*10^{16}*6.2*10^{16}}{(1.4*10^{10})^2} = 0.78\,\text{V},$$

b. d_p and d_n widths of both common d and p & n domains will be defined in the following way

$$d = \sqrt{\frac{2\varepsilon\varepsilon_0\varphi_k\left(N_d + N_a\right)}{qN_dN_a}} = \sqrt{\frac{2*12*8.86*10^{-14}*0.78*(4.8*10^{16}+6.2*10^{16})}{1.6*10^{-19}*4.8*10^{16}*6.2*10^{16}}} = 0.196\,\text{um}$$

$$\frac{d_n}{d_p} = \frac{N_a}{N_d} = \frac{p_p}{n_n}, \quad d_p = d - d_n,$$

$$d_n = \frac{d*N_a}{N_d(1+N_a/N_d)} = \frac{0.0000196*6.2*10^{16}}{4.8*10^{16}*\left(1+\frac{6.2*10^{16}}{4.8*10^{16}}\right)} = 0.11\text{um}$$

$$d_p = d - d_n = 0.196 - 0.11 = 0.086\,\text{um}$$

c. The maximum E_m strength of electrical field is defined by the following impression:

$$E_m = \frac{2*\varphi_k}{d} = \frac{2*0.78}{0.0000196} = 7.9*10^4\,\text{V/cm}$$

4b9.

a. j_S density of photodiode's saturation current by ideal p-n junction can be defined as follows:

At first from Einstein equation define diffusion coefficients of electrons and holes

$D_n = \frac{kT}{q}\mu_n = 0.026*1300 = 33.8$ cm²/v, $D_p = \frac{kT}{q}\mu_p = 0.026*500 = 13$ cm²/v, where kT/q=0.026V, then the densities of minority carriers.

$$p_n = \frac{(n_i)^2}{N_d} = \frac{(1.4*10^{10})^2}{10^{15}} = 1.96*10^5 \text{ cm}^{-3}, \quad n_p = \frac{(n_i)^2}{N_a} = \frac{(1.4*10^{10})^2}{5*10^{15}} = 3.9*10^4 \text{ cm}^{-3}$$

And finally the current density:

$$j_S = q\left(\frac{D_pP_n}{L_p} + \frac{D_nn_p}{L_n}\right) = 1.6*10^{-19}\left(\frac{13*1.96*10^5}{0.006} + \frac{33.8*3.9*10^4}{0.01}\right) = 8.8*10^{-11}\,\text{A/cm}^2$$

b. In order to define open circuit voltage, first define the photo current by the above mentioned values

$$I_f = q\alpha W\beta S\Phi = 1.6*10^{-19}*10^3*0.01*0.7*10^{-4}*10^{18} = 1.1*10^{-4}\,\text{A}$$

then open circuit voltage

$$V_{xx} = \frac{kT}{q}\ln\left(\frac{I_{ü}}{I_S}+1\right) \approx \frac{kT}{q}\ln\left(\frac{I_{ü}}{I_S}\right) = 0.026*\ln\left(\frac{1.1*10^{-4}}{8.8*10^{-11}}\right) = 0.3\,\text{V}$$

4b10.

a. Define h_1/h_2 ratio of h_1 and h_2 widths of the channel near the source and drain. Near source reverse biasing voltage applied on p-n junction $V_{p-n} = V_G + V_1 = 1 + 0.5 = 1.5\,\text{V}$, and near the drain $V_{p-n} = V_G + V_2 = 1 + 1 = 2\,\text{V}$. Near source width of charge layer $d_1 = \left(2\varepsilon\varepsilon_0\mu_n\rho V_{P-n}\right)^{1/2} = \left(2*12*8.85*10^{-14}*1300*0.5*1.5\right)^{1/2} = 0.45*10^{-4}$ cm, and near the drain

$$d_2 = \left(2\varepsilon\varepsilon_0\mu_n\rho V_{P-n}\right)^{1/2} = \left(2*12*8.85*10^{-14}*1300*0.5*2\right)^{1/2} = 0.52*10^{-4}\,\text{cm}.$$

h_1 and h_2 widths of source and drain of the channel will be defined:

$$h_1 = \alpha - 2d_1 = 2*10^{-4} - 2*0.45*10^{-4} = 1.1*10^{-4} \text{ cm},$$

$$h_2 = \alpha - 2d_2 = 2*10^{-4} - 2*0.52*10^{-4} = 0.96*10^{-4} \text{ cm},$$

Thus h_1/h_2 ratio of h_1 and h_2 widths will be

$$h_1/h_2 = 1.1/0.96 = 1.15$$

b. cutoff voltage

$$V_{G0} = \frac{\alpha^2}{8\varepsilon\varepsilon_0\mu_n\rho} = \frac{4*10^{-8}}{8*12*8.85*10^{-14}*1300*0.5} = 7.24\,\text{V}$$

4b11.

a. Define C capacitance of the gate in depletion mode

$$S = \ell \cdot b = 10^{-2}*10^{-2} = 10^{-4}\ \text{cm}^2 \qquad C = \frac{\varepsilon\varepsilon_0 S}{d} = \frac{12*8.85*10^{-14}*10^{-4}}{0.5*10^{-4}} = 2.12*10^{-12}\,\text{F}$$

b. In order to define the cutoff voltage, first find the density of majority carriers in the channel $n = N_C \exp\left[-\frac{E_C - E_F}{kT}\right] = 10^{19} * \exp\left[-\frac{0.2}{0.025}\right] = 3.2*10^{15}$ cm^{-3}, then the cutoff voltage

$$V_{G0} = \frac{qn\alpha bl}{C} = \frac{1.6*10^{-19}*3.2*10^{15}*2*10^{-4}*10^{-2}*10^{-2}}{2.12*10^{-12}} = 4.8\,\text{V}$$

4b12.

Capacitance of the abrupt p-n- junction is given by

$$C = \sqrt{\frac{\varepsilon\varepsilon_0 N_A N_D e}{2(N_a + N_0)(V_r + \varphi_k)}}S\,,$$

where N_A and N_D are the donor and acceptor densities and S is cross section area of diode.
When V_r=2 V, C_1=200 pF

$$C_1 = S\sqrt{\frac{\varepsilon\varepsilon_0 N_A N_D e}{2(N_a + N_0)(V_{r1} + \varphi_k)}}\,,$$

When reverse bias is V_r, then C_2 = 50 pF.

$$C_2 = S\sqrt{\frac{\varepsilon\varepsilon_0 N_A N_D e}{2(N_a + N_0)(V_{r2} + \varphi_k)}}\,,$$

Therefore

$$\frac{C_1}{C_2} = \sqrt{\frac{V_{r2} + \varphi_k}{V_{r1} + \varphi_k}}\,,$$

From this equation it follows

$$V_{r2} = \left(\frac{C_1}{C_2}\right)^2 (V_{r1} + \varphi_k) - \varphi_k = 44.1\ \text{V}.$$

4b13.

$$\sigma = e\mu_n N_D$$

$$N_D = \frac{\sigma}{e\mu_n} = 10^{21}\mu^{-3}$$

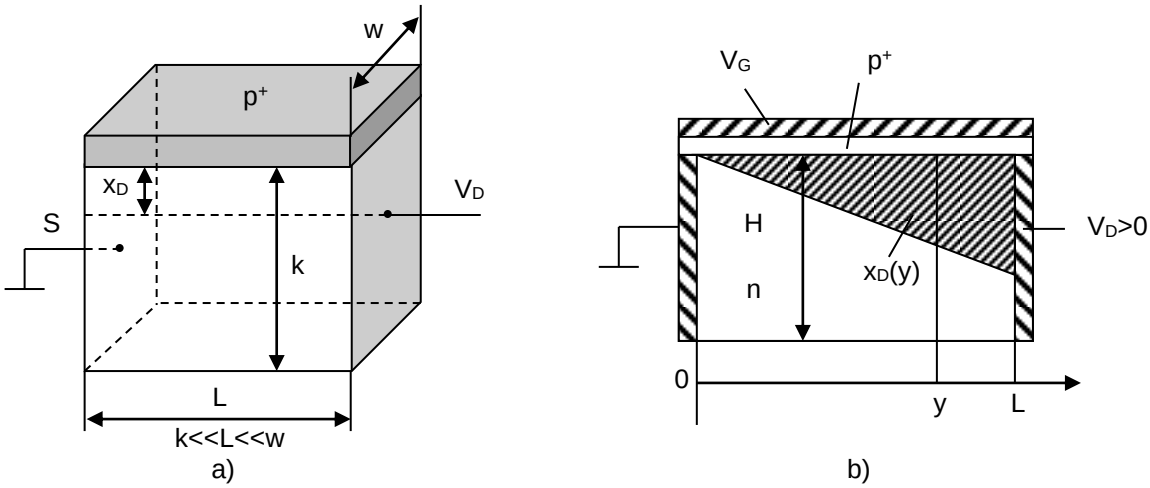
The “pinch-off” voltage of the channel for the abrupt p-n junction is

$$U_{po} = \frac{\varepsilon N_D a^2}{2\varepsilon\varepsilon_0}\,,$$

where $a = \frac{w}{2} = 4\ \mu$ m, hence

$$U_{po} = 12 \text{ V}.$$

4b14.
For the simplification asymmetric field effect transistor will be considered, the channel of which is an n-type semiconductor, and the gate is p^+-type region which forms the p^+-n junction with the channel.



The n-channel of the transistor has length L (a distance from source to drain), width w and depth H (a distance between the insulating substrate and metallurgical boundary of the gate).
When the source is grounded and V_D=0, the channel effective width (the width of its quasI-neutral part) is uniform in any cross section y=const and equals (H-x_D), where

$$x_D = \sqrt{\frac{2\varepsilon\varepsilon_0(V_{bi} - V_G)}{eN_D}}\ .$$

Here V_{bi} is the contact potential difference , V_G-gate voltage, N_D is the channel doping level, ε- dielectric , ε_0-electrical constant and e is an elementary charge.
Assume that p^+-region of the gate is strongly doped and therefore almost all space charge region can be considered as fully expanded in the n- channel region.
L>>H and the Schottky graduate channel approximation is valid. Also for the uniform doped channel the approximation of complete depletion layer is applicable. When V_D>0, the drain current in the y section is

$$I_D = eN_D w[H - x_D(y)]v(y),$$

where v(y)- is the electron drift velocity, which is defined by ε_y-component of electrical field in the section y:

$$v(y) = \frac{\mu_n \varepsilon_y}{1 + \frac{\varepsilon_y}{\varepsilon_c}},$$

and

$$x_D = \sqrt{\frac{2\varepsilon\varepsilon_0(V(y) + V_{bi} - V_G)}{eN_D}}$$

is depletion layer width in the same section.

As L>>H, then $\varepsilon_y = \frac{dV(y)}{dy}$, and

$$I_D = eN_D w\left[H - \sqrt{\frac{2\varepsilon\varepsilon_0(V(y) + V_{bi} - V_G)}{eV_D}}\right]\frac{\mu_n}{1 + \frac{1}{\varepsilon_c}\frac{dv}{dy}}\frac{dv}{dy}$$

or

$$I_D = \left\{ eN_D w \left[H - \sqrt{\frac{2\varepsilon\varepsilon_0 \left(V(y) + V_{bi} - V_G\right)}{eV_D}} \right] \mu_n - \frac{I_D}{\varepsilon_c} \right\} \frac{dv}{dy}$$

Integrating this equation y=0 (V(0)=0) up to y=L (V(L)=V_D), considering that I_D=Const, the following can be obtained:

$$I_D \cdot L = \int_0^{V_D} \left\{ eN_D w \left[H - \sqrt{\frac{2\varepsilon\varepsilon_0 \left(V(y) + V_{bi} - V_G\right)}{eV_D}} \right] \mu_n - \frac{I_D}{\varepsilon_c} \right\} dv =$$

,

$$= eN_D wH\mu_n V_D - eN_D w\mu_n \int_0^{V_D} \sqrt{\frac{2\varepsilon\varepsilon_0 \left(V(y) + V_{bi} - V_G\right)}{eV_D}} dv - \frac{I_D}{\varepsilon_c} V_D$$

Or

$$I_D \left(1 + \frac{V_D}{\varepsilon_c L} \right) = \frac{eN_D wH\mu_n V_D}{L} - \frac{eN_D w\mu_n}{L} \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_D}} \int_0^{V_D} \sqrt{V + V_{bi} - V_G}\, dv .$$

After some transformation the final expression for the drain current follows:

$$\frac{I_D}{I_p} = \frac{3\frac{V_D}{V_{bi} - V_T} - 2\left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_T} \right)^{\frac{3}{2}} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_T} \right)^{\frac{3}{2}} \right]}{1 + \frac{V_D}{\varepsilon_c L}},$$

where

$$I_p = \frac{3N_D wH\mu_n}{3L} \left(V_{bi} - V_T \right)$$

$$V_T = V_{bi} - \frac{eN_D H^2}{2\varepsilon\varepsilon_0} .$$

4b15.

For a “limited source” condition with the total amount of impurities Q, the solution of the Fick equation is given by the Gaussian function.

$$N(x,t) = \frac{Q}{\sqrt{\pi Dt}} \exp\left[-\left(\frac{x}{2\sqrt{Dt}} \right)^2 \right]$$

$p-n$ junction is forming at that place, where boron concentration equals to the concentration of impurities in the bulk silicon substrate, that is:

$$\frac{Q}{\sqrt{\pi Dt}} \exp\left[-\left(\frac{x_j}{2\sqrt{Dt}} \right)^2 \right] = N_D$$

Solving this equation with respect to x_j, the following is obtained

$$x_j = 2\sqrt{Dt} \sqrt{\ln\left[\frac{Q}{N_D \sqrt{\pi Dt}} \right]}$$

Substituting the numerical values of Q, D, N_D and t, into this expression yields

$$x_j = 2{,}7\ \mu\text{m}.$$

4b16.
First find equilibrium heights of emitter and collector junctions:

$$\varphi_{0E} = \frac{kT}{e}\ln\frac{N_{AE}\cdot N_{DB}}{n_i^2} = 0.856 \text{ eV},$$

$$\varphi_{0K} = \frac{kT}{e}\ln\frac{N_{DB}\cdot N_{AK}}{n_i^2} = 0.635 \text{eV}.$$

The width of emitter junction depletion region in the base of the transistor is

$$W_{nE} = \sqrt{\frac{2\varepsilon\varepsilon_0(e\varphi_{0E} - U_{EB})}{e^2 N_{DB}^2\left(\frac{1}{N_{AE}} + \frac{1}{N_{DB}}\right)}} = 0.215 \ \mu\text{m},$$

and correspondingly the width of collector junction depletion region in the base is

$$W_{nK} = \sqrt{\frac{2\varepsilon\varepsilon_0(e\varphi_{0K} - U_{BK})}{e^2 N_{DB}^2\left(\frac{1}{N_{AK}} + \frac{1}{N_{DB}}\right)}} = 0.258 \ \mu\text{m}.$$

Therefore the width of the neutral base will be equal

$$W_B = W - W_{nE} - W_{nK} = 0.527 \ \mu\text{m}.$$

The concentration of minority carries (holes) at the emitter-base junction will equal the following:

$$p_n(0) = \frac{n_i^2}{N_{DB}}\exp\left(\frac{eU_{EB}}{kT}\right) = 5.18\cdot 10^{12} \ cm^{-3}.$$

Finally, the total charge of minority carries accumulated in the base is

$$Q = \frac{eS\ p_n(0)W_B}{2} = 6.4\cdot 10^{-13} \ K.$$

4b17.

Bipolar diffusion coefficient is determined as

$$D = \frac{n+p}{\frac{n}{D_p} + \frac{p}{D_n}}.$$

For intrinsic semiconductor

$$D = \frac{2D_nD_p}{D_n + D_p}.$$

Using Einstein relations one obtains

$$D = \frac{k_BT}{e}\frac{2\mu_n\mu_p}{\mu_n + \mu_p} \approx 20{,}7 \text{ cm}^2/\text{s}.$$

4b18.
First a density of donors in the semiconductor can be defined:

$$N_D = \frac{1}{e\mu_n\rho} = 1.6\cdot 10^{15} \ cm^{-3}.$$

The built-in potential barrier for the electrons is equal to

$$\varphi_m = \Phi_{Au} - \Phi_{Ge},$$

Here the semiconductor work function can be represented as

$$\Phi_{Ge} = \chi_{Ge} + E_c - E_F = \chi_{Ge} + kT\ln\frac{N_c}{N_D} = \chi_{Ge} + kT\ln\frac{N_c}{n_i} + kT\ln\frac{n_i}{N_D} = \chi_{Ge} + \frac{E_g}{2} - \varphi_0$$

where it is meant, that

$$\frac{E_g}{2} = kT\ln\frac{N_c}{n_i},$$

and

$$\varphi_0 = kT\ln\frac{N_D}{n_i} = 0.11 \text{ eV}$$

Therefore, $\Phi_{Ge} = 4.22$ eV, and $\varphi_m = 0.78$ eV.

4b19.

a) $\gamma = \dfrac{I_{ep}}{I_{ep} + I_{en}} = \dfrac{3}{3 + 0.01} \approx 0.9967$,

b) $\alpha_T = \dfrac{I_{cp}}{I_{ep}} = \dfrac{2.99}{3} = 0.9967$,

c) $\alpha_0 = \gamma\alpha_T = 0.9934$

$I_e = I_{ep} + I_{en} = 3.01$ m²

$I_c = I_{cp} + I_{cn} = 2.99 + 0.001 = 2.991$ mA

$I_{c\mu 0} = I_c - \alpha_0 I_e = 2.991 - 0.9934 \cdot 3.01 = 0.000866 = 0.87$ uA.

4b20.

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_S q N_a (2\psi_B)}}{C_{ox}}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{d} = \frac{3.9 \cdot 8.85 \cdot 10^{-14}\,\text{F}}{5 \cdot 10^{-7}\,\text{cm} \cdot cm} = 6.9 \cdot 10^{-7}\,\text{F/cm}^2$$

$$V_{FB} = \psi_S - \frac{Q_{ox}}{C_{ox}} \approx -0.98 - \frac{1.6 \cdot 10^{-19} \cdot 5 \cdot 10^{11}}{6.9 \cdot 10^{-7}} \approx -1.1\,\text{V}$$

$$V_T = -1.1 + 0.84 - \frac{\sqrt{2 \cdot 11.9 \cdot 8.85 \cdot 10^{-14} \cdot 1.6 \cdot 10^{-19} \cdot 10^{17} \cdot 0.84}}{6.9 \cdot *10^{-7}} \approx 0.02\,\text{V}$$

The substrate accumulation charge (Boron) will lead to flat-band bias by $\dfrac{qN_{\text{bor}}}{C_{ox}}$, and therefore

$$0.6 = -0.02 + \frac{qN_{\text{µáñ}}}{C_{ox}}$$

$$N_{\text{µáñ}} = \frac{0.62 \cdot 6.9 \cdot 10^{-7}}{1.6 \cdot 10^{-19}} \approx 2.67 \cdot 10^{12}\,\text{cm}^{-2}$$

4b21.

$$\sigma_1 = \sigma_o e^{-\frac{\Delta E}{2kT_1}} \qquad \Delta\sigma = \sigma_1 - \sigma_2 = \sigma_0\left(e^{-\frac{\Delta E}{2kT_2}} - e^{-\frac{\Delta E}{2kT_1}}\right)$$

$$\sigma_2 = \sigma_o e^{-\frac{\Delta E}{2kT_2}} \qquad \frac{\Delta\sigma}{\sigma_1} = \frac{e^{-\frac{\Delta E}{2kT_2}} - e^{-\frac{\Delta E}{2kT_1}}}{e^{-\frac{\Delta E}{2kT_1}}} = e^{-\frac{\Delta E}{2k}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)} - 1 \approx 1.18 - 1 \approx 0.18$$

Answer: will increase by 18%.

4b22.

$$\sigma = en\mu_n + ep\mu_p \qquad p = \frac{n_i^2}{n}$$

$$\sigma = en\mu_n + e\frac{n_i^2}{n}\mu_p$$

Find the minimum value from $\frac{d\sigma}{dn} = 0$ condition:

$$\frac{d\sigma}{dn} = e\mu_n - e\frac{n_i^2}{n^2}\mu_p = 0$$

$$\mu_n = \frac{n_i^2}{n^2}\mu_p \Rightarrow n = n_i\sqrt{\frac{\mu_p}{\mu_n}}$$

$$p = \frac{n_i^2}{n} = \frac{n_i^2}{n_i\sqrt{\frac{\mu_p}{\mu_n}}} = n_i\sqrt{\frac{\mu_n}{\mu_p}}$$

4b23.

$$\mu = \frac{e\tau}{m};\ L_d = \sqrt{D\tau};\ D = \frac{kT}{e}\mu$$

$$L_d = \sqrt{\frac{kT}{e}\mu\tau} = \sqrt{\frac{kT\tau^2}{m}} = \tau\sqrt{\frac{kT}{m}}$$

$$L_D - \frac{L_D}{10} = \sqrt{\frac{kT}{e}\mu\left(1+\frac{1}{20}\right)\cdot\tau\left(1+\frac{x}{100}\right)} = \sqrt{\frac{kT\tau^2}{m}\left(1+\frac{1}{20}\right)\cdot\left(1+\frac{x}{100}\right)}$$

$$L_D\left(1+\frac{1}{10}\right) = \tau\sqrt{\frac{kT}{m}\left(1+\frac{1}{20}\right)\cdot\left(1+\frac{x}{100}\right)} = \sqrt{\frac{21}{20}\cdot\frac{100+x}{100}}$$

Answer: will increase by 15%.

4b24.

a. using Bohr model, the ionization energy of donors in any semiconductor is expressed by:

$$E_d = \left(\frac{\varepsilon_o}{\varepsilon_s}\right)^2 \cdot \left(\frac{m^*}{m_o}\right) \cdot E_H$$

$$E_d = \frac{1}{(17)^2} \cdot 0.014 \cdot 13.6 \approx 6.58 \cdot 10^{-4}$$ eV

b. The radius of the first orbit (n=1) is connected to the corresponding radius of hydrogen atom

$$r = \left(\frac{\varepsilon \cdot m_o}{m^*}\right) r_H$$

$$r_{I_nS_b} = \left(\frac{17}{0.014}\right) \cdot 0.53 = 643.6 \overset{o}{A}$$

c. density of conducting electrons

$$n \approx \frac{N_d}{1 + g \exp\left(-\frac{E_d}{kT}\right)} \approx \frac{N_d}{1 + 2\exp\left(-\frac{E_d}{kT}\right)}$$

$$kT = 0.00034$$

$$n = \frac{1 \cdot 10^{14}}{1 + 2\exp(-2)} = 0.78x10^{14}$$

4b25.

Field tension in space

For metal

$$E = \frac{V_k}{d} = 10^7$$ V/cm.

Surface density of charge

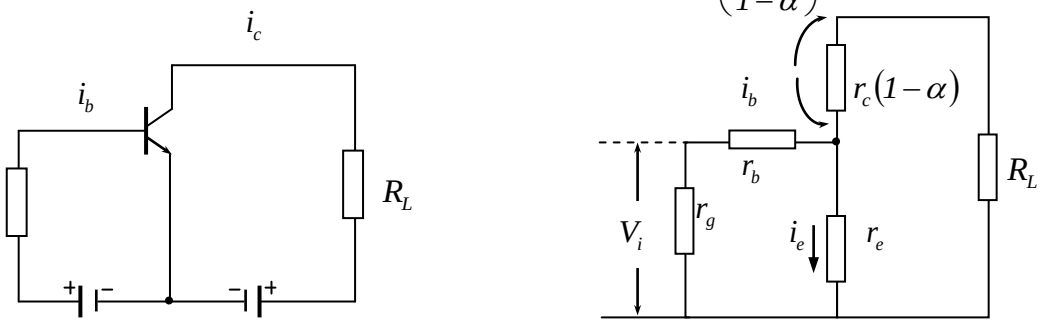
$$Q_s = E_k \cdot \varepsilon_o,\ Q_s = 10^7 \cdot 8.85 \cdot 10^{-14} = 8.85 \cdot 10^7$$ K/cm²

Number of electrons $n = \frac{Q_s}{q} = \frac{8.85 \cdot 10^{-7}}{1.6 \cdot 10^{-19} K} \cdot \frac{K}{cm^2} \approx 5.5 \cdot 10^{12} cm^{-2}$

in order to provide the difference of the same potentials (for metal–n type semiconductor contact) it will be necessary to deplete $W = \frac{n}{n_{ss}} = \frac{5 \cdot 10^{12}}{10^{15}} = 5 \cdot 10^{-3}$ cm width layer from semiconductor.

4b26.

According to AC, the input voltage



$$V_i = i_e r_e + i_b r_b$$

$$\alpha = i_c / i_e ,$$

$$i_b = (1-\alpha) i_e$$

Input power

$$P_i = V_i \cdot i_b = \left[i_e r_e + (1-\alpha) \cdot i_e r_b \right] (1-\alpha) i_e$$

Output power

$$P_{out} = i_c^2 R_L = i_e^2 \alpha R_L$$

Amplification coefficient according to power

$$G_p = \frac{\alpha^2 R_L}{\left[r_e + (1-\alpha) r_b \right] (1-\alpha)}$$

$\alpha = 0.98,\ r_e = 20$ Ohm, $r_b = 500$ Ohm, $R_L \approx 30$ kOhm

$$G_p = \frac{0.98^2 \cdot 3 \cdot 10^4}{(20 + 0.02 \cdot 500)(0.02)} = 5 \cdot 10^4$$

4b27.

As it is known $n \sim T^{3/2} \exp(-E_g / 2k_B T)$. Therefore

$\frac{n_1}{n_2} = \left(\frac{T_1}{T_2} \right)^{3/2} \exp\left[-\frac{E_g(0)}{2k_B} \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right]$, where $E_g = E_g(0) - \alpha T$. Therefore

$$E_g(0) = 2k_B \frac{T_1 T_2}{T_1 - T_2} \ln\left(n_1 T_2^{3/2} / n_2 T_1^{3/2} \right) = 0.26$$ Ev.

4b28.

In the given case continuity equation has the following form: $D_p \frac{d^2 \Delta p}{dx^2} - E \mu_p \frac{d \Delta p}{dx} - \frac{\Delta p}{\tau_p} = 0$, $x \neq 0$, or

$$\frac{d^2 \Delta p}{dx^2} - \frac{eE}{k_B T} \frac{d \Delta p}{dx} - \frac{\Delta p}{L_p^2} = 0 :$$

It is obvious that $\Delta p \to 0$, when $x \to \pm\infty$. Therefore

$$\Delta p = \begin{cases} \Delta p(x=0)\exp(k_1 x), & \mathrm{x} < 0 \\ \Delta p(x=0)\exp(k_2 x), & \mathrm{x} > 0 \end{cases}$$

where $k_{1,2} = eE/2k_BT \pm \left(e^2E^2/4k_B^2T^2 + L_p^{-2}\right)^{1/2}$. It is obvious that $k_1 > 0$ and $k_2 < 0$.

4b29.

From the determination of the injection coefficient it follows that $j_p(0) = \xi\left[j_p(0) + j_n(0)\right]$. Therefore $j_n(0) = j_p(0)(1-\xi)/\xi$. Hole current density at $x = 0$ equals $j_p(0) = -eD_p \left.\frac{d\Delta p}{dx}\right|_{x=0}$. Taking into account that in the considered case $\Delta p = \Delta p(x=0)\exp(-x/L_p)$, one obtains $j_p(0) = eD_p\Delta p(0)/L_p$. Therefore $j_n(0) = eD_p\Delta p(0)(1-\xi)/\xi L_p = 1.68$ mA.cm^{-2}.

4b30.

Sample resistivity $\rho = RS/l = 0.03$ Ohm. On the other hand, $\rho = 1/(en\mu_n + ep\mu_p) = 1/(e\frac{n_i^2}{p}\mu_n + ep\mu_p)$. Hence $p = \frac{1+\sqrt{1-4e^2\rho^2\mu_n\mu_p n_i^2}}{2e\rho\mu_n} = 4\times10^{21}$ m^{-3}.

4b31.

a. The density of radiation, coming to surface is F, and in d depth, after absorption, is $Fe^{-\alpha d}$. Therefore, the number of quantum, absorbed in d depth, is $F\left(1-e^{-\alpha d}\right)$, and the photocurrent, occurred in the result of absorption, is $I_{Ph}=qSF(1-e^{-\alpha d})$.

b. Find the photocurrent, occurred in the result of absorption of λ_1 wave radiation. $I_{Ph1} = qSF\left(1-e^{-\alpha_1 d}\right) \approx 10^{-9}$A.

c. Find the photocurrent, occurred in the result of absorption of λ_2 wave radiation.

$$I_{Ph2} = qSF\left(1-e^{-\alpha_2 d}\right) \approx 0.15.10^{-9}\text{A}$$

d. Find the ratio of photocurrents.

$$\frac{I_{Ph1}}{I_{Ph2}} \approx 6.7$$

4b32.

In general, the performance of photodiode is characterized by three processes 1. τ_{RC} time constant, 2. τ_d diffusion time of non-equilibrium charges through the base and 3. τ time of non-equilibrium charges through bulk charge domain.

Time constant of photodiode is defined by base resistance and charge capacitance of p-n junction. $\tau_{RC} = RC$:

Base resistance and charge capacitance of p-n junction are defined by the following expressions:

$$R = \frac{w}{Sqn\mu_n} \approx 0{,}3 \text{ Ohm}, \quad C = \frac{S\varepsilon\varepsilon_0}{d} \approx 10^{-10}\text{F}.$$

Therefore, $\tau_{RC} = RC \approx 3\cdot10^{-11}$s.

Diffusion time of non-equilibrium charges through the base can be defined by the following expression: $\tau_d = w^2/2D = 2{,}9\cdot10^{-7}$s.

The drift time of non-equilibrium charges through bulk charge domain can be defined by the following expression:

$$\tau = \frac{d}{V_{max}} = 2 \cdot 10^{-11} \text{s}.$$

Therefore, photodiode performance, which is defined by the largest time constant, in the given case diffusion time of non-equilibrium charges through the base, will equal $2{,}9 \cdot 10^{-7}$s.

4b33.
In order to define the power density equivalent to the noise of photodiode, its basic noise must be taken into account, which has fluctuation nature and is defined by average square value of current fluctuation by the following expression:

$$\bar{I}_{dr}^2 = 2qI\Delta f,$$

as well as photosensitivity, according to power, by the following expression:

$$S_i(\lambda) = \frac{I_L}{P}:$$

Consider that minimum signal, detected against the background of noise is defined by the value of signal noise ratio, equal to one.

$$\frac{I}{\sqrt{\bar{I}_{dr}^2}} \equiv \frac{S_i(\lambda)P}{\sqrt{\bar{I}_{dr}^2}} = 1:$$

Threshold sensitivity can be defined, i.e. the minimum power of radiation which will be detected against the background of the noise.

$$P = \frac{\sqrt{\bar{I}_{dr}^2}}{S_i(\lambda)}$$

$\bar{I}^2$ is proportional to Δf range of bandwidth, hence, the power density, equivalent to noise in the unit layer of frequency will be.

$$P = \frac{1}{S_i(\lambda)} \sqrt{\frac{\bar{I}_{dr}^2}{S\Delta f}} = 8 \cdot 10^{-12} \text{ Vt} \cdot \text{Hz}^{-1/2} \cdot \text{cm}^{-1}$$

4b34.
Near the source, d width of p-n junction will be defined by the following expression:

$$d_1 = \left(\frac{2\varepsilon\varepsilon_0}{q} . \frac{\varphi}{N_d} \right)^{1/2} = 0{,}36 \cdot 10^{-4} \text{cm}.$$

and near the drain:

$$d_2 = \left(\frac{2\varepsilon\varepsilon_0}{q} . \frac{\varphi_{\breve{I}} + V}{N_d} \right)^{1/2} = 1{,}79 \cdot 10^{-4} \text{ cm}.$$

therefore narrowing size of channel near the source will equal $d_1 - d_2 = 1{,}43 \cdot 10^{-5}$cm.

5. SEMICONDUCTOR TECHNOLOGY

a) Test questions

5a1. E
5a2. D
5a3. D
5a4. D
5a5. B
5a6. C
5a7. B
5a8. B
5a9. B
5a10. A
5a11. B
5a12. B
5a13. C
5a14. A
5a15. B
5a16. D
5a17. C
5a18. D
5a19. C
5a20. C
5a21. B
5a22. C
5a23. B
5a24. C
5a25. B
5a26. A
5a27. E
5a28. D
5a30. C
5a31. A
5a32. A
5a33. C
5a34. A
5a35. B
5a36. D
5a37. B
5a38. C
5a39. A

b) Problems

5b1.

$\rho_p=10^{-4}$ Ohm·m
$\rho_n=10^{-2}$ Ohm·m
$\mu_p=0,05\ m^2\ V^{-1}\ s^{-1}$
$\mu_n=0,13\ m^2\ V^{-1}\ s^{-1}$
$n_i=1,38x10^{16}\ m^{-3}$
T=300K
φ_c =?

The contact potential is obtained from $\varphi_c= (kT/q)\ln p_p/p_n=0,0258\ \ln p_p/p_n$
The densities of holes and electrons are obtained using the specific resistance expressions:

$$P_P = \frac{1}{\rho_P q \mu_P} = \frac{1}{10^{-4} \cdot 1,6 \cdot 10^{-19} \cdot 0,05} = 1,25 \cdot 10^{24}\ m^{-3}$$

$$n_n = \frac{1}{\rho_n q \mu_n} = \frac{1}{10^{-2} \cdot 1,6 \cdot 10^{-19} \cdot 0,13} = 4,2 \cdot 10^{21}\ m^{-3}$$

The holes' density in n region is obtained using the mass action law:

$$P_n = \frac{n_i^2}{n_n} = \frac{2 \cdot 10^{32}}{4{,}2 \cdot 10^{21}} = 4{,}8 \cdot 10^{10}\ \text{m}^{-3}$$

The contact potential of p–n junction

φ_c=0,0258 Inp_p/p_n=In1,25x10^{24}/4,8x10^{10}=0,8V.

5b2.

σ_p=100 S/cm
μ_p=1900 $cm^2 V^{-1} s^{-1}$
T=300 K
n_i =2,5x10^{13} atom/cm^3
p_p , n_p=?
Using the expression of the specific conductance
$\sigma_p=1/q\mu_p p_p$, the holes' density

$$p_p = \frac{\sigma_p}{q\mu_p} = \frac{100}{1{,}6 \cdot 10^{-19} \cdot 1900} = 3{,}29 \cdot 10^{17}\ \text{cm}^{-3}$$

The concentration of electrons is obtained using the mass action law:

$n_p\ p_p = n_i^2$.

$$n_p = \frac{n_i^{\ 2}}{p_p} = \frac{6{,}25 \cdot 10^{26}}{3{,}29 \cdot 10^{17}} = 1{,}9 \cdot 10^{9}\ \text{cm}^{-3}$$

5b3.

N_d= 10^{17}atom/cm^3
L=100 μm
W=10 μm
d=1 μm
μ_n= 1500 $cm^2 V^{-1} s^{-1}$
T=300K
R and ρ_s= ?
Assuming that the impurities are fully ionized, the electrons concentration n =N_d
The specific resistance

$\rho_n = 1/\sigma = 1/qn\mu_n$, ρ_n=1/1,6x10^{-19}x10^{17}x1500= 0,042 Ohm·cm

The resistance

$R=\rho_n L/ W{\cdot}d$ =0,042 x100·10^{-4} /10x10^{-4}x1x10^{-4}=4,2 kOhm.

The sheet resistance

$\rho_s=\rho_n/ d$ = 0,042/1x10^{-4}= 420 Ohm/mm.

5b4.

C_{0x}=100 nF/cm^2=100x10^{-9} F/cm^2
ε_{SiO2}=3,9x8,85x10^{-14} F/cm
t_{ox}= ?
Calculate the thickness of SiO_2 layer by the intrinsic formula of MOS-capacitor's permittivity.

$C_{0x}= \varepsilon_{SiO2}/ t_{ox}$ and $t_{ox}= \varepsilon_{SiO2}/ C_{0x}$

t_{ox}=3,9x8,85x10^{-14} /100x10^{-9}

t_{ox}=3,45x10^{-6} cm=0,0345 um.

To grow the high quality gate oxide, the dry oxidation process will be used.

5b5.

The gate capacitance is defined as

$$C = C_{ox}S = (\varepsilon_0 \varepsilon_{ox} / t_{ox})WL$$

After the scaling by the α factor

$$C_{sc} = (\varepsilon_0 \varepsilon_{ox} / t_{ox} / \alpha)\,(W/\alpha)L/\alpha) = (\varepsilon_0 \varepsilon_{ox} / t_{ox})WL / \alpha = C/\alpha\ .$$

For α=2, $C_{sc}= C/2$.

The capacitance will decrease by factor two.

5b6.
For direct voltage, the current density:

when T=T_1 $j_1 \to exp\left(-\frac{E_g - qV}{kT_1}\right) = exp\left(-\frac{0.7 - 0.4 \cdot 1.6 \cdot 10^{-19}}{0.022}\right) = 1.2 * 10^{-6}$ A/cm^2.

when T=T_2 $j_2 \to exp\left(-\frac{E_g - qV}{kT_2}\right) = exp\left(-\frac{0.7 - 0.4 \cdot 1.6 \cdot 10^{-19}}{0.026}\right) = 9.7 * 10^{-6}$ A/cm^2.

therefore $\frac{j_2}{j_1}$ =8.08.

5b7.
Near the drain, the width of p-n junction when the voltage applied to drain is V = 0.1V:

$$d_1=\left(\frac{2\varepsilon\varepsilon_0}{q}.\frac{\varphi_i + V}{N_1}\right)^{1/2} = \left(\frac{2 \cdot 12 \cdot 8.86 \cdot 10^{-14}}{1.6 \cdot 10^{-19}} \cdot \frac{0.6 + 0.1}{10^{15}}\right)^{1/2} = 9.64 \cdot 10^{-5} \text{ cm}$$

and in case of voltage absence:

$$d_2=\left(\frac{2\varepsilon\varepsilon_0}{q}.\frac{\varphi_i}{N_1}\right)^{1/2} = 8.93 \cdot 10^{-5} \text{cm}$$

therefore, near the drain, the channel will narrow by $d_1-d_2=0.71 \cdot 10^{-5}$cm.

5b8.
Saturation voltage of the transistor

$$V_{DSsat.} = V_{GS} - V_t = 3\text{-}1 = 2\text{V}.$$
$$V_{DS} > V_{DS\ sat}$$

therefore the transistor operates in saturation mode. In this mode the drain current of the transistor equals:

$$I_D = 0{,}5\ \mu_n\ Cox\ (W/L)\ (V_{GS} - V_t)^2.$$

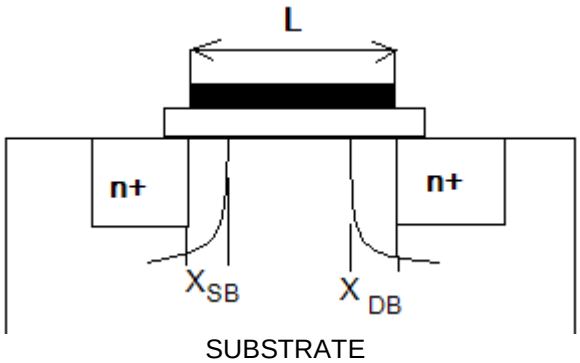
Calculate

$$Cox = (\varepsilon_0\ \varepsilon_{si\ o2})/\ t_{ox} = (3{,}9x8{,}85x10^{-14})/10x10^{-7} = 3{,}45x10^{-7}\ F/cm^2.$$
$$I_D = 0{,}5x300x3{,}45x10^{-7}(3\text{-}1)^2x\ (10/1) = 2{,}07\ mA.$$

Transconductance $g_m = d\ I_D/d\ V_{GS}$

$$g_m = \mu_n\ Cox\ (W/L)\ (V_{GS} - V_t) = 300x3{,}45x10^{-7}x10\ x2 = 2\ mA$$

5b9.



SUBSTRATE

$$L_{эф} = L - X_{SB}(V_S) - X_{DB}(V_D)$$

By data, L_{eff} =0, hence

$$X_{DB}(V_D) = L - X_{SB}(V_S)$$

Use the width formula of depletion region:

$$2\varepsilon_0\,\varepsilon_{Si}\,(\varphi_i - V_D)/q\,N_{sub} = (L - X_{SB}(0))^2$$

$$V_D=\varphi_c - q\,N_{sub}(L - X_{SB}(0))^2/\,2\varepsilon_0\,\varepsilon_{Si}$$

Calculate

$$\varphi_c = \varphi_T \ln N_{sub}\,N_{don}/\,n_i^2$$

In a room temperature

$$\varphi_T \approx 0{,}026\ V \text{ and } \varphi_c \approx 0{,}935\ V.$$

$$X_{SB}(0)=\sqrt{2\varepsilon_0\,\varepsilon_{Si}\,\varphi_c / q\,N_{sub}}$$

$$X_{SB}(0)= \sqrt{2x\ 8{,}85x10\text{-}14x11{,}8x0{,}935/1{,}6x10^{-19}x10^{16}}$$

$$X_{SB}(0) \approx 0{,}349x10^{-4}\ cm.$$

Put and calculate

$$|V_D| \approx 2{,}3\ V.$$

5b10.

Density of electronic current

$$J_n = eD_n\,dN/dx$$

According to Einstein formula:

$$D_n = \varphi_T\ \mu_n, \text{ and } dN/dx = k$$

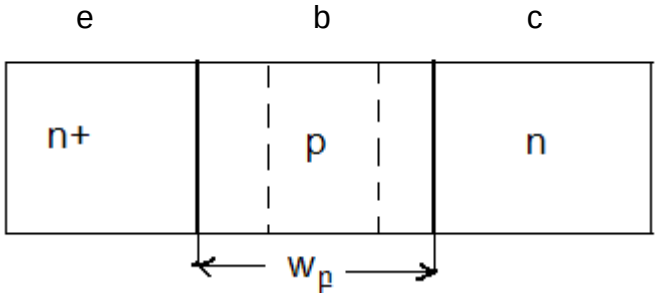
$$J_n = e\ \varphi_T\ \mu_n\ k$$

In a room temperature

$$\varphi_T = 0{,}026\ V$$

$$J_n = 1{,}6\ 10^{-19}\ x\ 0{,}026\ x1200\ x\ 8\ x\ 10^{18} = 39{,}936\ A/cm^2$$

5b11.



a. Calculate the difference of contact potentials in E-B and C-B p-n junctions. At a room temperature

$$\varphi_T \approx 0{,}026\ V$$

$$\varphi_{ce} = \varphi_T \ln N_e\,N_b/\,n_i^2 \quad \varphi_{ce=}\ 0{,}026\ \ln 10^{19}x10^{15}/2{,}25x10^{20} \approx 0{,}8759\ V$$

$$\varphi_{cc} = \varphi_T \ln N_b N_c/\,n_i^2 \quad \varphi_{cc} = 0{,}026\ \ln 10^{16}x5x10^{15}/2{,}25x10^{20} \approx 0{,}7\ V$$

b. Calculate E-B depletion layer width when the external voltage =0.

$$X_{eb}(0)=\sqrt{2\varepsilon_0\,\varepsilon_{Si}\,\varphi_{ce} / q\,N_b} \approx 3{,}38x10^{-5}cm = 0{,}338\ um.$$

c. For base punch-through, X_{cb} depletion layer width must be

$$X_{cb} = 0{,}6 - 0{,}338 = 0{,}262\ um.$$

d. The voltage of the collector can be obtained from the following equation:

$$X_{cb} = \sqrt{2\varepsilon_0\,\varepsilon_{Si}\,N_c\,(\varphi_{cc}-V) / q\,N_b\,(N_b + N_c)}.$$

Hence

$$V = \varphi_{cc} - X^2_{cb}\,q\,N_b\,(N_b + N_c)\,/2\varepsilon_0\,\varepsilon_{Si}\,N_c \quad \text{and} \quad |V| \approx 0{,}8765\ V$$

6. NUMERICAL METHODS AND OPTIMIZATION

a) Test questions

6a1. E
6a2. D
6a3. D
6a4. B
6a5. B
6a6. A
6a7. A
6a8. B
6a9. A
6a10. A
6a11. A
6a12. C
6a13. C
6a14. D
6a15. C
6a16. A
6a17. D
6a18. D
6a19. B
6a20. B
6a21. B
6a22. A
6a23. A
6a24. D
6a25. C
6a26. E
6a27. D
6a28. C
6a29. C
6a30. B
6a31. D
6a32. D
6a33. E
6a34. A
6a35. A
6a36. D
6a37. B
6a38. D
6a39. C
6a40. D
6a41. B
6a42. D
6a43. B
6a44. D
6a45. A
6a46. A
6a47. A
6a48. C
6a49. D
6a50. A
6a51. B
6a52. C
6a53. D
6a54. B
6a55. B
6a56. A
6a57. B
6a58. C
6a59. D
6a60. A
6a61. B
6a62. C
6a63. B

b) Problems

6b1.

Define low and upper values of the game and their corresponding optimal strategies. There is:

$$\alpha = \max_i \min_j h_{ij}\text{ , }\alpha=2,\ i=3,\ j=1;$$

$$\beta = \max_j \min_i h_{ij}\text{ , }\beta=3,\ i=1,\ j=1:$$

As $\alpha\neq\beta$, i.e. there is mixed strategy matrix game in case of which vector elements of $P=(p_1,p_2,p_3)^T$ probabilities are the probabilities of selecting A side corresponding strategy. $Q=(q_1,q_2,q_3)^T$ vector elements are the ones of selecting B side corresponding strategy.

$$\alpha\le V\le\beta,$$

$$\begin{cases} 3p_1 - p_2 + 2p_3 \ge V, \\ -2p_1 + 4p_2 + 2p_3 \ge V, \\ 4p_1 + 2p_2 + 6p_3 \ge V, \\ p_1 + p_2 + p_3 = 1, \end{cases} \qquad \begin{cases} 3q_1 - 2q_2 + 4q_3 \le V, \\ -q_1 + 4q_2 + 2q_3 \le V, \\ 2q_1 + 2q_2 + 6q_3 \le V, \\ q_1 + q_2 + q_3 = 1, \end{cases}$$

In the result of solving the system the following is obtained:

$p_1=0$, $p_2=0$, $p_3=1$;
$q_1=2/5$, $q_2=3/5$, $q_3=0$;
$V=2$.

6b2.
Define $\Phi(t, t_0)$ by matrix method.
There is:

$$M\left(A(t)\right)_{3x3} = E_{3x3} + Q^1\left(A(t)\right)_{3x3} =$$

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} + \begin{bmatrix} \int_2^1 t dt & \int_2^1 t^2 dt & \int_2^1 t^3 dt \\ \int_2^1 1 dt & \int_2^1 t dt & \int_2^1 (2-t) dt \\ \int_2^1 t^2 dt & \int_2^1 t dt & \int_2^1 t dt \end{bmatrix} = \begin{bmatrix} \left(\frac{t^2}{2} - 1\right) & \left(\frac{t^3}{3} - \frac{8}{3}\right) & \left(\frac{t^4}{4} - 4\right) \\ (t-1) & \left(\frac{t^2}{2} - 1\right) & \left(2t - \frac{t^2}{2} - 2\right) \\ \left(\frac{t^3}{3} - \frac{8}{3}\right) & \left(\frac{t^2}{2} - 2\right) & (t-1) \end{bmatrix} = \Phi(t, t_0):$$

6b3.
There is

$$H = \begin{bmatrix} 0 & 0.4472 & 0.4851 \\ 0 & 0 & 0.4851 \\ 1 & 0.8944 & 0.7276 \end{bmatrix},$$

The opposite of which

$$H^{-1} = \begin{bmatrix} -2 & 0.5 & 1 \\ 2.2361 & -2.2361 & 0 \\ 0 & 2.0616 & 0 \end{bmatrix}.$$

Therefore

$$\Phi(t) = H \cdot diag\left(e^{-\lambda_i}\right) \cdot H^{-1} = \begin{bmatrix} e^{-2t} & \left(-e^{-2t} + e^{-3t}\right) & 0 \\ 0 & e^{-3t} & 0 \\ 2\left(e^{-2t} - e^{-t}\right) & \left(\frac{1}{2}e^{-t}\, 2e^{-2t} + \frac{3}{2}e^{-3t}\right) & e^{t} \end{bmatrix}.$$

6b4.
There is

λ_1=4.4142, λ_2=1.5858, λ_3=0;

$$H = \begin{bmatrix} -0.3366 & -0.5615 & -0.2182 \\ -0.4760 & 0.7941 & -0.8729 \\ -0.8125 & 0.2326 & 0.4364 \end{bmatrix},\ H^{-1} = \begin{bmatrix} -0.6731 & -0.2380 & -0.8125 \\ -1.1230 & 0.3971 & 0.2326 \\ -0.6547 & -0.6547 & 0.6547 \end{bmatrix}.$$

Therefore

$$diag(A) = H \cdot A \cdot H^{-1} = \begin{bmatrix} 4.4142 & 0 & 0 \\ 0 & 1.5858 & 0 \\ 0 & 0 & 0 \end{bmatrix}.$$

6b5.
As the constant term of characteristic polynomial (P3) is equal to the determinant of matrix, therefore it will be

$$P_3 = det\begin{bmatrix} 1 & -2 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix} = 1\cdot 1\cdot 1 + 2\cdot 2 = 5.$$

6b6.
As

$$\|A\|_2 = \left(\sum_{i=1}^{3}\sum_{j=1}^{3} a_{ij}^2 \right)^{1/2}$$

then

$$\|A\|_2 = \sqrt{1^2 + (-2)^2 + 1^2 + 2^2 + (-1)^2 + 1^2} = \sqrt{12}$$

6b7.

As coefficient of characteristic polynomial term containing λ^2 is $P_1 = -\sum_{i=1}^{3}\lambda_i$,

$$P_1 = -(1+2+3) = -6:$$

6b8.
As characteristic polynomial coefficient of the term which contains λ^2

$$P_1 = \sum_{i,j=1}^{4}\lambda_i \cdot \lambda_j ,$$

then

$$P_2 = \lambda_1\lambda_2 + \lambda_1\lambda_3 + \lambda_1\lambda_4 + \lambda_2\lambda_3 + \lambda_2\lambda_4 + \lambda_3\lambda_4 = 0\cdot 1 + 0\cdot 2 + 0\cdot 3 + 1\cdot 2 + 1\cdot 3 + 2\cdot 3 = 11.$$

6b9.
It is known that linear interpolation error is defined by the following formula:

$$R_2 = \frac{1}{8} M_2 h^2 ,$$

Where h is the length of the step, $M_2 = \max_{x\in[0,1000]} |f''(x)|$. As $f(x) = \log x$, then $M_2 = 1$. Therefore, in order to provide the necessary accuracy, h should be taken $\sqrt{0.008} \approx 0.089$.
Taking into consideration that $f''(x) = -x^{-2}$, i.e. for large x-es the derivative is small, then dividing the range into parts, it is possible to enlarge division step. For example, divide $[0,1000]$ range into $[0,10],[10,100],[100,1000]$ ranges. In that case, h_1 division step in the 1st range equals 0.089 (as $M_{2,1} = \max_{x\in[0,10]} |f''(x)| = M_2 = 1$). In the 2nd range $M_{2,2} = 0.01$, therefore, h_2 step is defined from $\frac{1}{8}\cdot 0.01\cdot h_2^2 < 0.001$ non-equation, i.e. $h_2 = 0.894$. Similarly, in the 3rd range $M_{2,3} = 0.0001$, and the step equals $h_3 = 8.94$. Thus, in order to provide the anticipated accuracy it is necessary to take approximately 100 points in each part. Other types of divisions of initial range can also be observed. The minimum number of points can be obtained by changing length of the next length in each step, i.e. in k th step h_k is selected by the following formula: $8^{-1}\,|x_k|^{-2}\,h_k^2 < 0.001$, $x_{k+1} = x_k + h_k$.

6b10.

The formula of generalized trapeziums, applied for the given integral, has the following view: $\frac{h}{2}\left(\frac{1}{b^2}+\frac{e}{1+b^2}+2\sum_{i=1}^{n-1}\frac{e^{x_i}}{x_i^2+b^2}\right)$. In the given case the error is defined by inaccuracy formula of generalized trapeziums' formula $\frac{M_2}{12}(1-0)h^2$, where $h=x_{i+1}-x_i$ - $[0,1]$ is interval division step. Noticing $M_2=O\left(b^{-4}\right)$, it is seen that the given formula does not operate in case of small b-s. Therefore, for $O\left(h^2\right)$ class provision it is necessary to divide $[0,1]$ part into subparts and to use smaller division step in 0 range. For example, by dividing $[0,1]$ into two subparts - $[0,l]$ and $[l,1]$, h_1 division step in the first range should be selected in a way that $h_1\approx hb^2$, and in the second range $h_2\approx h\left(l^2+b^2\right)$. Other forms of division can also be discussed.

6b11.

As $\frac{f(x)}{\sqrt{x}}$ function has uniqueness in 0 point, it is not possible to apply squarization formula at once. For that reason divide $[0,1]$ part into $[0,10^{-8}]$ and $[10^{-8},1]$ ranges. The integral with the first range allows $\left|\int_0^{10^{-8}}\frac{f(x)}{\sqrt{x}}dx\right|=|f(c)|\cdot 2\sqrt{10^{-8}}\approx C\cdot 10^{-4}$ mark ($0<c<10^{-8}$). This mark allows ignoring the first integral and calculating only the integral with the second range, where the integrating function has no uniqueness and therefore, squarization formulas is possible to apply. But as $\sqrt{x}$ accepts small values in that range, it is desirable to improve the integrating function in advance by using integration in parts formula $\int_{10^{-8}}^{1}\frac{f(x)}{\sqrt{x}}dx=\int_{10^{-8}}^{1}f(x)d2\sqrt{x}=2f(1)-2f\left(10^{-8}\right)10^{-4}-\int_{10^{-8}}^{1}2\sqrt{x}f'(x)dx$. For the final integral, the formula of generalized rectangular can be applied, the error of which is estimated by $M_1\frac{h}{4}\left(1-10^{-8}\right)$ formula where $M_1\le m_1\cdot 10^2$ ($m_1=\max_{x\in[0,1]}|f'(x)|$). In the last inequality $|f''(x)|\le 1$ condition has been used. Eventually, $h\approx 10^{-6}$.

6b12.

Notice that $x^3-20x+1=0$ equation is solved which has three $z_1<z_2<z_3$ real roots. Write the formula of iteration process in the following view $x_{n+1}-x_n=\frac{x_n^3-20x_n+1}{20}$. From this it follows that in $x_0<z_1$ or $x_0>z_3$ case, the method diverges (the difference in the left part is monotonous); $x_0=z_1$ and $x_0=z_3$ points are static; in $z_1<x_0<z_3$ case the method converges z_2.

6b13.

The constants α and β cannot be found uniquely, because the term 'smallest error' is not defined in the formulation of problem. First, it must be defined exactly what 'the smallest error' means. For example, the distance between functions f and g can be defined as $\|f-g\|=\max_{x\in[-10,10]}|f(x)+g(x)|$ (uniform norm). In this case the best approximating linear function will be $y=2.5$ (it follows from Chebyshev theorem). On the other hand, the function $y=\frac{arctg100}{20}\approx\frac{\pi}{40}$ gives the best approximation, when the distance

between functions f and g is defined as $\|f-g\|_2=\sqrt{\int_{-10}^{10}|f(x)-g(x)|^2\,dx}$ (root-mean-square norm). Also the weighting norms $\|f-g\|_{2,p}=\sqrt{\int_{-10}^{10}|f(x)-g(x)|^2\,p(x)dx}$ may be considered where the weighting function p is a fixed positive function. In this case the coefficients α,β will depend on p.

6b14.

The integration interval is not bounded; therefore, the multiple-application rectangle rule cannot be applied immediately. Assume the function f on interval $[1,\infty)$ is bounded by the constant C: $|f(x)|\le C$. The integral can be represented in this form:

$$\int_1^{\infty}\frac{f(x)dx}{1+x^2}=\int_1^{1.5C\varepsilon^{-1}}\frac{f(x)dx}{1+x^2}+\int_{1.5C\varepsilon^{-1}}^{3C\varepsilon^{-1}}\frac{f(x)dx}{1+x^2}+\int_{3C\varepsilon^{-1}}^{\infty}\frac{f(x)dx}{1+x^2}\equiv I_1+I_2+I_3$$

The estimate of the function f implies inequalities $|I_2|<\frac{\varepsilon}{3}$ and $|I_3|<\frac{\varepsilon}{3}$. Applying multiple-application rectangle rule for the first integral, this is obtained:

$$I_1\approx\tilde{I}_1=h\sum_{k=1}^{N}\frac{f(x_k)}{1+x_k^2},\ \text{where}\ N=\frac{1.5C}{h\varepsilon}.$$

The reminder term of this formula is the following:

$$R_1=\frac{M_1(1.5C-\varepsilon)h}{2\varepsilon},\ \text{where}\ M_1=\max_{x\ge1}\left|\left(\frac{f(x)}{1+x^2}\right)'\right|$$

Hence for $h=\frac{4\varepsilon^2}{9CM_1}$ the necessary accuracy is obtained:

$$\left|\int_1^{\infty}\frac{f(x)dx}{1+x^2}-\tilde{I}_1\right|<\varepsilon.$$

Notice that the obtained step h is too small, so in this case non-equidistant intervals can be used. The rectangle rule for non-equidistant intervals takes this form

$$\tilde{I}_2=\sum_{k=1}^{N}\frac{f(x_k)}{1+x_k^2}(x_{k+1}-x_k),$$

with the reminder term

$$R_1=\sum_{k-1}^{N}\frac{M_k(x_{k+1}-x_k)^2}{2}$$

Taking into account that

$$M_k=\max_{x\in[x_k,x_{k+1}]}\left|\left(\frac{f(x)}{1+x^2}\right)'\right|\le\frac{M}{x_k^2}+\frac{C}{x_k^4},\ \text{where}\ M=\max_{x\ge1}|f'(x)|,$$

this is obtained

$$R_1\le\frac{M_0}{2}\sum_{k=1}^{N}\frac{1}{x_k^2}(x_{k+1}-x_k)^2,\ \text{where}\ M_0=\max(M,C).$$

Thus, taking the partition points x_k so that $R_1<\frac{\varepsilon}{3}$, the final formula is obtained.

6b15.

The polynomial P_3 is represented as

$P_3(x)=(a_0+a_1(x-x_1))(x-x_2)^2+(a_2+a_3(x-x_2))(x-x_1)^2\equiv P_{3,1}(x)+P_{3,2}(x)$. The advantage of this representation is the following. For the function $P_{3,k}$ there is $P_{3,k}(x_j)=P'_{3,k}(x_j)=0$ where $j\neq k$, $j,k=1,2$. Using the conditions $P_3^{(k)}(x_1)=P_{3,1}^{(k)}(x_1)=f^{(k)}(x_1)$, where $k=0,1$, $a_0=\dfrac{f(x_1)}{(x_2-x_1)^2}$, $a_1=\dfrac{f'(x_1)}{(x_1-x_2)^2}-\dfrac{2f(x_1)}{(x_1-x_2)^3}$ is obtained. The same formulas exist for a_2 and a_3. Finally, the polynomial P_3 is presented as follows:

$$P_3(x)=\left(f(x_1)+\left(f_1'(x_1)-\frac{2f(x_1)}{x_1-x_2}\right)(x-x_1)\right)\frac{(x-x_2)^2}{(x_1-x_2)^2.}+$$
$$+\left(f(x_2)+\left(f_2'(x_2)-\frac{2f(x_2)}{x_2-x_1}\right)(x-x_2)\right)\frac{(x-x_1)^2}{(x_2-x_1)^2}$$

Using the same considerations the needed formula can be obtained for arbitrary number of the points x_k.

6b16.

There are many ways to solve this problem. For example, using successive approximations $x_{k+1}=\dfrac{x_k^4+1}{10}$, $x_0=0$, the root of the equation on the interval $[0,1]$ with prescribed accuracy can be found after four steps. If the bisection method on the same interval is used, seven steps will be necessary.

6b17.

Substituting $t=x-1$, the problem is reduced to the equivalent problem of definition of quadratic function $G(t)=a_1t^2+b_1t+c_1$, which gives the best approximation for the function

$$F(t)=\frac{1}{2+t}+\frac{1}{2-t}$$

in $[-1,1]$ interval. Taking into account, that F function is even in symmetric interval, and defining distance between two functions as $D_1=\max\limits_{[-1,1]}|F(t)-G(t)|$, or $D_2=\int\limits_{-1}^{1}(F(t)-G(t))^2\,dt$, $b_1=0$ is obtained. Consider, for example, D_1 distance case. It is represented it in this form:

$$D_1=\max_{[-1,1]}|F(t)-G(t)|=\max_{t\in[-1,1]}\left|\frac{4}{4-t^2}-a_1t^2-c_1\right|=\max_{z\in[0,1]}\left|\frac{4}{4-z}-a_1z-c_1\right|.$$

As the function $\dfrac{4}{4-z}$ is convex in $[0,1]$ interval and denoting $L=\min\limits_{a_1,c_1}D_1$, the system for the definition of the best approximation polynomial of first order is obtained.

$$\begin{cases}\dfrac{4}{4-0}-c_1=L\\ \dfrac{4}{4-1}-a_1-c_1=L\\ \dfrac{4}{(4-z_0)^2}-a_1=0\\ \dfrac{4}{4-z_0}-a_1z_0-c_1=-L\end{cases}$$

Here $0, z_0, 1$ points are Chebyshev's alternance points. Solving that system this is obtained:

$$a_1 = \frac{1}{3},\ \ c_1 = \frac{4\sqrt{3}-1}{6},\ \ L = \frac{7-4\sqrt{3}}{6}.$$

So, the best approximation polynomial will be $y = \frac{1}{3}(x-1)^2 + \frac{4\sqrt{3}-1}{6}$, with minimal distance $L = \min D_1 = \frac{7-4\sqrt{3}}{6} \approx 0.012$.

The case of distance D_2 is easier. Also, one can consider the case of weighted approximation, when $D_\rho = \int_{-1}^{1} (F(t)-G(t))^2 \rho(t)dt$, where ρ is the given positive function.

6b18.

Calculating Δ_n, $\Delta_{n+1} = 2\Delta_n - \Delta_{n-1}$ recurrent formula for $n > 1$ is obtained. Solving it, $\Delta_n = C_1 + C_2 n$ is obtained, where C_1 and C_2 are unknown constants. As $\Delta_1 = 2$ and $\Delta_2 = 3$, $\Delta_n = n+1$. So, $\lim_{n\to\infty} \frac{\Delta_n}{n} = 1$ is obtained.

6b19.

One of possible ways. Assume the equation of AB line is $l(x,y) \equiv ax + by + c = 0$. This line splits the plane into two half-planes: $\{(x,y) : l(x,y) > 0\}$ and $\{(x,y) : l(x,y) < 0\}$. If the point D lies in triangle's interior, then substituting the coordinates of that and C point into $l(x,y)$, values of the same sign will be obtained (i.e. D and C belong to the same half-plane). The same considerations can be done for BC and AC lines. An arbitrary polygon case can be reduced to triangle case by partitioning and checking if D point lies in one of partition triangles.

6b20.

The polynomial P_4 is represented in this form:

$$P_4 = (x-x_2)\left(a_0 + a_1(x-x_1) + a_2(x-x_1)^2 + a_3(x-x_1)^3\right) + (x-x_1)^4 b_0.$$

Substituting that polynomial into the given equalities, the system for determination of unknown a_k and b_0 is obtained:

$$(x_2-x_1)^4 b_0 = y_4,\ \begin{cases} (x_1-x_2)a_0 = y_0 \\ a_0 + (x_1-x_2)a_1 = y_1 \\ 2a_1 + 2(x_1-x_2)a_2 = y_2 \\ 6a_2 + 6(x_1-x_2)a_3 = y_3 \end{cases}.$$

The general case may be considered analogously.

6b21.

As characteristic polynomial's absolute term (P_3) equals to determinant of matrix, then it will be

$$P_3 = det\begin{bmatrix} 1 & -3 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix} = 1\cdot 1\cdot 1 + 3\cdot 2 = 7.$$

6b22.
As

$$\|A\|_2 = \left(\sum_{i=1}^{3} \sum_{j=1}^{3} a_{ij}^2 \right)^{1/2} = \sqrt{1^2 + (-3)^2 + 1^2 + 2^2 + (-1)^2 + 1^2} = \sqrt{17}\,.$$

6b23.
As the coefficient of first degree of λ in the characteristic polynomial

$$P_1 = \sum_{i=1}^{3} \lambda_i\,,$$

then

$$P_1 = 1 + 4 + 2 = 7:$$

6b24.
A As the coefficient of first degree of λ^2 in the characteristic polynomial

$$P_1 = \sum_{i,j=1}^{4} \lambda_i \cdot \lambda_j\,,$$

then

$$P_2 = \lambda_1\lambda_2 + \lambda_1\lambda_3 + \lambda_1\lambda_4 + \lambda_2\lambda_3 + \lambda_2\lambda_4 + \lambda_3\lambda_4 = 4\cdot 1 + 4\cdot 2 + 4\cdot 3 + 1\cdot 2 + 1\cdot 3 + 2\cdot 3 = 35$$

6b25.
We have five linearly independent conditions for determination of the P_n polynomial coefficients. Therefore, the minimal value of n for which the problem has a solution for arbitrary values y_j and z_k cannot be less than four. Forth order polynomial which satisfies given conditions, can be found explicitly, similar to Lagrange interpolation polynomial. First, we find basic polynomials Φ_j and Ψ_k, satisfying conditions

$$\Phi_j^{(i)}(1) = \delta_{ij},\ i = 0,1,2\,, \qquad \Phi_j^{(q)}(0) = 0,\ \ q = 0,1\,, \qquad \text{for } j = 0,1,2$$
$$\Psi_k^{(i)}(1) = 0,\ i = 0,1,2\,, \qquad \Psi_k^{(q)}(0) = \delta_{kq},\ \ q = 0,1 \qquad \text{for } k = 0,1.$$

Here δ_{ij} is a Kronecker symbol ($\delta_{ij} = 0$ for $i \neq j$ and $\delta_{ii} = 1$). After that, the required polynomial is found by the formula

$$P_4(x) = \sum_{j=0}^{2} y_j \Phi_j(x) + z_0 \Psi_0(x) + z_1 \Psi_1(x).$$

Let us show how to construct basic polynomials. Consider, for example, Φ_1.
We will search this polynomial in the form

$$\Phi_1(x) = x^2(x-1)\big(a(x-1) + b\big).$$

Then the constants a, b will be determined from the conditions $\Phi_1'(1) = 1,\ \Phi_1''(1) = 0$, or $b = 1,\ 2a + 4b = 0$, from which we have $a = -2,\ b = 1$. The remaining basic polynomials can be found analogously.

The polynomials P_4 can be found also directly, by writing down it in the form $P_4(x) = x^2\big(a(x-1)^2 + b(x-1) + c\big) + (x-1)^3(dx + e)$, and determining coefficients a, b, c, d, e from problem conditions by constants y_j and z_k.

6b26.
As the function $f(x) = x^3$ is odd, and an interval $[-1,1]$ is symmetric relative to origin, then the required polynomial have to be odd function, too. Hence, $P_1(x) = ax$, where the constant a must be determined.

For the determination of this constant we consider the function $g(x)=f(x)-P_1(x)=x^3-ax$ on the interval $[0,1]$. We have $g(0)=0$ and $g(1)=1-a$. The function g is convex, therefore a can be found from the condition, that the minimal value of function g at some point x_0 of open interval $(0,1)$ is equal to $g(1)=1-a$ with opposite sign. Then in the interval $[-1,1]$ we will get four points ($z_1=-1, z_2=-x_0, z_3=x_0, z_4=1$), where $f(z_k)-P_1(z_k)=(-1)^k\|f-P_1\|$, so, by the Chebyshev theorem, the polynomial $P_1=ax$ will be the required polynomial of best approximation. So: $g'(x)=3x^2-a$, from which $x_0=\sqrt{\frac{a}{3}}$. Further, $g\left(\sqrt{\frac{a}{3}}\right)=-\frac{2}{3}a\sqrt{\frac{a}{3}}$, and therefore the constant a can be found from equation $1-a=\frac{2}{3}a\sqrt{\frac{a}{3}}$. Solving this equation, we get $a=\frac{3}{4}$. Finally, the polynomial of best approximation is $P_1(x)=\frac{3}{4}x$. This problem can be solved easier, using geometric considerations.

6b27.

Assume λ is eigenvalue of A matrix. In that case $\det(A-\lambda E)=0$ (E is unit matrix). If A matrix satisfies $A^n=0$ condition, where n is a natural number, then we have

$-\lambda^n E=A^n-\lambda^n E=(A-\lambda E)(A^{n-1}+\lambda A^{n-2}+\lambda^2 A^{n-3}+\ldots+\lambda^{n-1}E)$,

therefore, using the properties of determinants

$-\lambda^n=\det(-\lambda^{n-1}E)=\det(A-\lambda E)\det(A^{n-1}+\lambda A^{n-2}+\lambda^2 A^{n-3}+\ldots+\lambda^{n-1}E)=0$

i.e. $\lambda=0$. Thus if $A^n=0$, where n is a natural number, then the eigenvalue of A matrix, equal zero.

6b28.

Substituting 1- in the expansion of the logarithm function we get alternating series $\ln 2=\sum_{k=1}^{\infty}(-1)^{k+1}\frac{1}{k}$. That series converges very slowly as, according to Leibniz theorem, $|\ln 2-S_N|\le\frac{1}{N+1}$, where S_N is a partial sum of the given series. Therefore, in order to provide the necessary accuracy it is necessary to take not less than 1000 terms of the series which leads to significant increase of round-off error. Therefore it is better to apply the following method. Define t number from equation $\frac{1+t}{1-t}=2$. We get $t=\frac{1}{3}$, hence, the seeking number is presented as:

$$\ln 2=\ln\left(1+\frac{1}{3}\right)-\ln\left(1-\frac{1}{3}\right)=\sum_{k=0}^{\infty}\left((-1)^{k+1}+1\right)\frac{1}{k3^k}$$

This series in the right part may be estimated by geometrical progression with $\frac{1}{3}$ quotient. Therefore in order t provide the necessary accuracy it is enough to take only 8 summands of the given series. The same method may be applied again. Other methods are also possible.

6b29.

As the absolute term (P_3) of characteristic polynomial equals to determinant of matrix, then it will be

$$P_3 = \det\begin{bmatrix} 2 & -6 & 0 \\ 0 & 2 & 4 \\ -2 & 0 & 2 \end{bmatrix} = 2\cdot 2\cdot 2 + (-6)\cdot(-2)\cdot 4 = 56:$$

6b30.

As the coefficient of λ^2 in the characteristic polynomial is equal to $P_2 = \sum_{\substack{i,j=1 \\ i\neq j}}^{4} \lambda_i \cdot \lambda_j$, then

$$\begin{aligned} P_2 &= \lambda_1\lambda_2 + \lambda_1\lambda_3 + \lambda_1\lambda_4 + \lambda_2\lambda_3 + \lambda_2\lambda_4 + \lambda_3\lambda_4 = \\ &= 2\cdot 0.5 + 2\cdot 1 + 2\cdot 1.5 + 0.5\cdot 1 + 0.5\cdot 1.5 + 1\cdot 1.5 = \\ &= 1 + 2 + 3 + 0.5 + 0.75 + 1.5 = 8.75: \end{aligned}$$

6b31.

As the characteristic equation looks as follows,

$$|\lambda E - A| = \begin{bmatrix} \lambda+2 & 0 \\ -1 & \lambda+1 \end{bmatrix} = (\lambda+1)\cdot(\lambda+2) = \lambda^2 + 3\lambda + 2 = 0,$$

the eigenvalues $\lambda_1 = -2, \lambda_2 = -1.$ The eigenvector, which corresponds to λ_1, has to be found from the homogeneous linear system $h_1 = (h_{11}, h_{21})^T$:

$$\begin{bmatrix} -2 & 0 \\ 1 & -1 \end{bmatrix} \cdot \begin{pmatrix} h_{11} \\ h_{21} \end{pmatrix} = -2 \cdot \begin{pmatrix} h_{11} \\ h_{21} \end{pmatrix},$$

and in the same way, the eigenvector $h_2 = (h_{12}, h_{22})^T$, which corresponds to λ_2, may be found from

$$\begin{bmatrix} -2 & 0 \\ 1 & -1 \end{bmatrix} \cdot \begin{pmatrix} h_{12} \\ h_{22} \end{pmatrix} = -1 \cdot \begin{pmatrix} h_{12} \\ h_{22} \end{pmatrix},$$

hence $h_{12} = 0,$ and for h_{22}, $h_{22} = 1$ can be chosen.
Solving these systems, the following is obtained:

$$\begin{pmatrix} h_{11} \\ h_{21} \end{pmatrix} = \begin{pmatrix} -1 \\ 1 \end{pmatrix} \begin{pmatrix} h_{12} \\ h_{22} \end{pmatrix} = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$$

So we will have transform matrix

$$H = \begin{bmatrix} -1 & 0 \\ 1 & 1 \end{bmatrix}$$

matrix for which $H^{-1} \equiv H$.

Finally $\Phi(t) = H \cdot \begin{bmatrix} e^{\lambda_1 t} & 0 \\ 0 & e^{\lambda_2 t} \end{bmatrix} \cdot H^{-1} = \begin{bmatrix} e^{-2t} & 0 \\ e^{-t} - e^{-2t} & e^{-t} \end{bmatrix}.$

$$\Phi(t) = \begin{bmatrix} e^{-2t} & 0 \\ e^{-t} - e^{-2t} & e^{-t} \end{bmatrix}$$

6b32.

It is obvious that

$$B = \begin{bmatrix} 0 & 0.5 \\ 0.5 & 0 \\ 0.5 & 1 \end{bmatrix}, \; A\cdot B = \begin{bmatrix} 0.5 & 1.25 \\ 0.25 & 0.25 \\ 0.5 & 0.5 \end{bmatrix}, \; A^2\cdot B = \begin{bmatrix} 0.75 & 1.125 \\ 0.375 & 0.75 \\ 0.375 & 0.375 \end{bmatrix}:$$

Therefore

$$\text{rang}L_x = \text{rang}[B \vdots AB \vdots A^2B] = \left[\begin{array}{cc:cc:cc} 0 & 0.5 & 0.5 & 1.25 & 0.75 & 1.125 \\ 0.5 & 0 & 0.25 & 0.25 & 0.375 & 0.75 \\ 0.5 & 1 & 0.5 & 0.5 & 0.375 & 0.375 \end{array}\right] = 3,$$

then the system is fully controllable.

7. DISCRETE MATHEMATICS AND THEORY OF COMBINATIONS

a) Test questions

7a1. E
7a2. A
7a3. B
7a4. A
7a6. A
7a7. C
7a8. E
7a9. E
7a10. D
7a11. C
7a12. D
7a13. A
7a14. B
7a15. A
7a16. C
7a17. D
7a18. D
7a19. E
7a20. A
7a21. E
7a22. A
7a23. B
7a24. B
7a25. E
7a26. D
7a27. B
7a28. C
7a29. E
7a30. A
7a31. E
7a32. D
7a33. E
7a34. B
7a35. A
7a36. C
7a37. D
7a38. B
7a39. A
7a40. B
7a41. C
7a42. B
7a43. B
7a44. C
7a45. B

b) Problems

7b1.

As $\xi_1=w$, $\xi_2=w$, $\xi_3=w$, but $\xi_1+\xi_2=w$, $\xi_1+\xi_3=w$ and $\xi_2+\xi_3=w$, therefore the corresponding threshold function will be:

$$x_1x_2\vee x_1x_3\vee x_2x_3,$$

to get Zhegalkin polynomial of which it is enough to use the following equation:

$$a\vee b=a\oplus b\oplus ab,$$

$$x_1x_2\vee x_1x_3\vee x_2x_3=(x_1x_2\oplus x_1x_3\oplus x_1x_2x_3)\vee x_2x_3=x_1x_2\oplus x_1x_3\oplus x_1x_2x_3\oplus x_2x_3\oplus(x_1x_2\oplus x_1x_3\oplus x_1x_2x_3)*$$
$$*x_2x_3=x_1x_2\oplus x_1x_3\oplus x_1x_2x_3\oplus x_2x_3\oplus x_1x_2x_3\oplus x_2x_3\oplus x_1x_2x_3\oplus x_1x_2x_3=x_1x_2\oplus x_1x_3\oplus x_2x_3:$$

7b2.

To verify the wholeness of the system it is enough to use Post theorem, i.e. find out if the system is fully included in any of classes of T_0, T_1, S, M, L?

- It is not included in T_0 as $x_1\to x_2\notin T_0$;
- It is not included in T_1 as $x_1x_2\overline{x_3}\notin T_1$;
- It is not included in S as $x_1\vee x_2\notin S$ (the functions depending on two variables are not self-dual at all);
- It is not included in M as $x_1\to x_2\notin M$ (00 set proceeds 10 set, whereas $0\to0=1$ and $1\to0=0$, i.e. monotony condition is violated);
- It is not included in L as $x_1\oplus x_2\oplus x_1x_2$ function is $x_1\vee x_2$ Zhegalkin polynomial and contains sum of variables, i.e. it is not linear - $x_1\vee x_2\notin L$

According to Post theorem, the system is complete.

7b3.

It is clear $\bar{x}\notin T_0$, $\bar{x}\notin T$, $1\notin S$ (as its table consists only of 1s and self-duality condition is violated – anti-symmetry towards middle line), $\bar{x}\notin M$ (as $0\not<1$, but $\bar{0}>\bar{1}$), $(x_1\to x_2)\to x_3\notin L$, as $a\to b=\bar{a}\vee b$, therefore $(x_1\to x_2)\to x_3=(x_1\vee x_2)\to x_3=\overline{\overline{x_1}\vee x_2}\vee x_3=x_1\overline{x_2}\vee x_3$, and from $a\vee b=a\oplus b\oplus ab$

equation it follows that $x_1\overline{x_2} \vee x_3 = x_1x_2 \oplus x_3 \oplus x_1\overline{x_2}x_3 =$
$= x_1(1 \oplus x_2) \oplus x_3 \oplus x_1x_3(1 \oplus x_2) = x_1 \oplus x_1x_2 \oplus x_3 \oplus x_1x_3 \oplus x_2x_3 \notin L$.
According to Post theorem, the system is complete.

7b4.
Search the solution in the form of indefinite coefficients.

x_1	x_2	x_3	$(x_1 \to x_2)^{\overline{x_3}}$
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$(x_1 \to x_2)^{\overline{x_3}} = a_0 \oplus a_1x_1 \oplus a_2x_2 \oplus a_3x_3 \oplus a_{12}x_1x_2 \oplus a_{13}x_1x_3 \oplus a_{23}x_2x_3 \oplus a_{123}x_1x_2x_3$
$1 = a_0$
$0 = a_3 \oplus 1$, $a_3 = 1$
$1 = 1 \oplus a_2$, $a_2 = 0$
$0 = 1 \oplus 1 \oplus a_{23}$, $a_{23} = 0$
$0 = 1 \oplus a_1$, $a_1 = 1$
$1 = 1 \oplus 1 \oplus 1 \oplus a_{13}$, $a_{13} = 0$
$1 = 1 \oplus 1 \oplus a_{12}$, $a_{12} = 1$
$0 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus a_{123}$, $a_{123} = 0$
Answer $1 \oplus x_1 \oplus x_3 \oplus x_1x_2$.

7b5.
Applying “divide to own” standard tactics, it is possible to get the solution of the problem by the following method:
a. by counting the number of units in couples
b. by summing couples
c. by counting the number of units in tetrads
d. by summing tetrads
e. the same continues for objects, 16-bit, 32-bit and other sequences
f. at the end of the process the number contains the number of units.

An example of solution for 16-bit number:

```
Count (n)
        n = (n & 0x5555) + ((n >> 1) & 0x5555)
        n = (n & 0x3333) + ((n >> 2) & 0x3333)
        n = (n & 0x0F0F) + ((n >> 4) & 0x0F0F)
        n = (n & 0x00FF) + ((n >> 8) & 0x0F0F)
return n;
```

7b6.
Taking into consideration binary arithmetic property, that N&(N-1) reduces the amount of units in the number by 1, which follows from the fact that N-1 makes all zeros at the end of the number into 1, and junior class unit - 0,leaving all high classes without change. Now, applying this action in the cycle, the amount of units in the number can be counted.

```
Count (n)
        C = 0;
        while (n <> 0)
                n = (n&(n-1))
                C = C + 1
        Return C
```

7b7.
Applying partition procedure, which is applied in QuickSort family algorithms, it is possible to get the following linear algorithm:

```
select(a, k, left, right)
        pivotNewIndex = partition(a, left, right, pivotIndex)
        while (k <> pivotNewIndex)
                if k < pivotNewIndex
                        right = pivotNewIndex-1
                 else
                        left = pivotNewIndex + 1
                pivotNewIndex = partition(a, left, right, pivotIndex)
        return k;
```

7b8.
Heap building is implemented in O(NlogN) period of time. Accordingly, applying the following algorithm, the elements can be classified in O(NlogN) period of time. The first (minimum or maximum) element is selected, substituted by the latter, after which the last element is shifted down its position in the heap, using ShiftDown standard procedure which requires O(logN) time. Applying N-1 procedure, sorted array in O(NlogN) period of time is obtained.

7b9.
Disjunctive normal form of this function having the mentioned table will be:

$$f = \overline{x}_1\overline{x}_2\overline{x}_3 \vee \overline{x}_1\overline{x}_2x_3 \vee \overline{x}_1x_2x_3 \vee x_1\overline{x}_2\overline{x}_3 \vee x_1x_2\overline{x}_3 \vee x_1x_2x_3$$

x_1	x_2	x_3	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Applying the first part of Qwine algorithm (“assembling”), the following will be obtained:
$\overline{x}_1\overline{x}_2\overline{x}_3 \vee \overline{x}_1\overline{x}_2x_3 \vee \overline{x}_1x_2x_3 \vee x_1\overline{x}_2\overline{x}_3 \vee x_1x_2\overline{x}_3 \vee x_1x_2x_3 \vee \overline{x}_1\overline{x}_2 \vee \overline{x}_2\overline{x}_3 \vee \overline{x}_1x_3 \vee x_2x_3 \vee x_1\overline{x}_3 \vee x_1x_2$
Applying the second part of Qwine algorithm (“absorption”), the following will be obtained:
$\overline{x}_1\overline{x}_2 \vee \overline{x}_2\overline{x}_3 \vee \overline{x}_1x_3 \vee x_2x_3 \vee x_1\overline{x}_3 \vee x_1x_2$

7b10.
Search Zhegalkin polynomial in the following form:

$$f(x_1,x_2,x_3) = a_0 \oplus a_1x_1 \oplus a_2x_2 \oplus a_3x_3 \oplus a_{12}x_1x_2 \oplus a_{13}x_1x_3 \oplus a_{23}x_2x_3 \oplus a_{123}x_1x_2x_3$$

x_1	x_2	x_3	$f(x_1,x_2,x_3)$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Substituting the right and left parts of the equation, sequentially all the possible values to x_1, x_2 and x_3 variables, this will be obtained:

$1=a_0$
$1=1\oplus a_3$, $a_3=0$
$1=1\oplus a_2$, $a_2=0$
$1=1\oplus 1\oplus a_{23}$, $a_{23}=1$
$1=1\oplus a_1$, $a_1=0$
$1=1\oplus a_{13}$, $a_{13}=0$

$1=1\oplus 1\oplus a_{12}$, $a_{12}=0$

$1=1\oplus 1\oplus 1\oplus a_{123}$, $a_{123}=0$

Putting the obtained values of the coefficients, Zhegalkin polynomial of the function will be obtained.

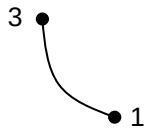
$$f(x_1,x_2,x_3)=1\oplus x_2\oplus x_2x_3$$

7b11.

As the length of Cayley h(G)=(3,5,4,4,5,6,7,8) vertex is equal 8, therefore the number of tree nodes equals 8+2=10. The numbers of those nodes are:

(1,2,3,4,5,6,7,8,9,10)

From those numbers choose the number from the left which is missing in Cayley code. That number is 1. Connect the node of 1 number with number one node of the vertex by edge.

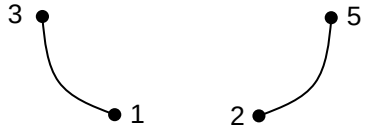


Delete 1 and 3 from the list of the number of nodes and vertex. The following will be obtained.

(1,2,3,4,5,6,7,8,9,10)

(3,5,4,4,5,6,7,8)

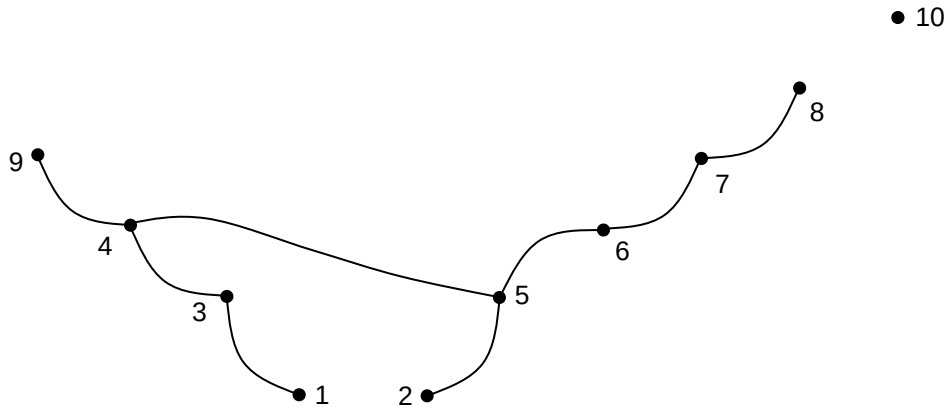
Do the same action after delete with the numbers of nodes and those numbers of nodes written in the code. This time connect the nodes of 2 and 5 numbers by edge and 2 and 5 numbers will be deleted from the list. This will be obtained:



(1,2,3,4,5,6,7,8,9,10)

(3,5,4,4,5,6,7,8)

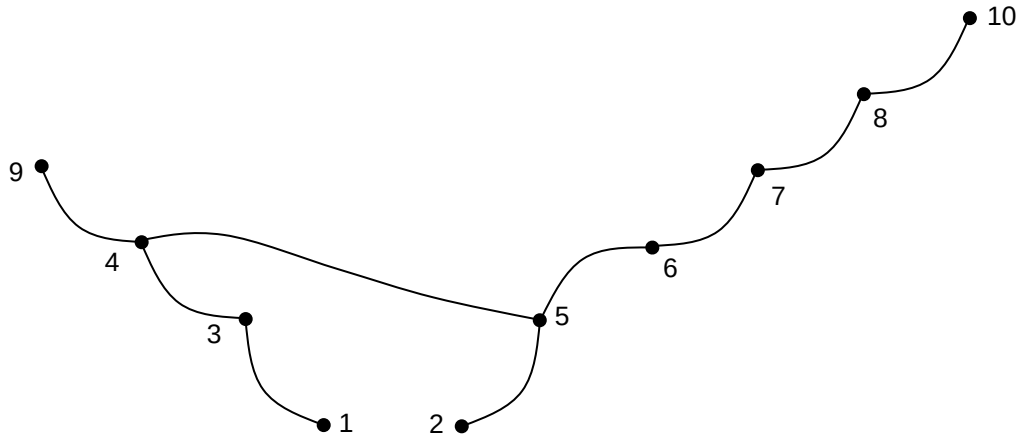
Continuing this action in the 8th step, this will be obtained



(1,2,3,4,5,6,7,8,9,10)

(3,5,4,4,5,6,7,8)

The last, final step is the connection of nodes with 8 and 10 numbers.



7b12.

x_1	x_2	x_3	$x_1^{x_2} \vee x_2^{x_3}$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

$x_1^{x_2} \vee x_2^{x_3} \notin S$, as the table is not antisymmetric.

$x_1\bar{x}_2 \notin M$, as for (1,0) and (1,1) the monotony condition is violated.

$x_1 \to x_2 \notin T_0$, as $0 \to 0 = 1$.

$x_1\bar{x}_2 \notin T_1$, as $1 \cdot \bar{1} = 0$.

$x_1\bar{x}_2 \notin L$, as $x_1\bar{x}_2 = x_1 \oplus x_1x_2$.

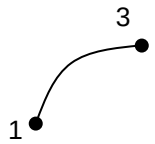
The system is complete.

7b13.

As the code length equals 8, therefore the number of tree nodes equals 10. The numbers of those nodes and tree code are:

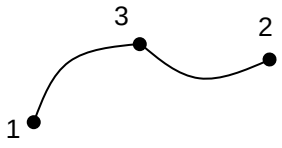
(1,2,3,4,5,6,7,8,9,10)
(3,2,4,4,5,6,8,8)

From those numbers choose the number from left to right which is missing in the code. It is 1. Connect the node of that number with number one node of the code from the left and delete those two numbers. The following will be obtained:



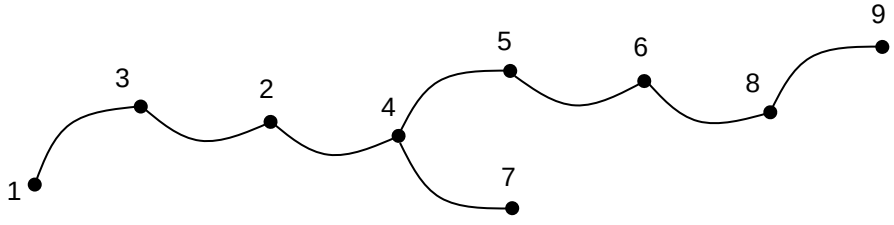
(1,2,3,4,5,6,7,8,9,10)
(3,2,4,4,5,6,7,8)

Apply the same process sequentially towards the obtained results. Once more the first number of the node from the left, which is missing in the code is 3. Connect the node of 3 number with the recurrent number of the node 3 and delete the two nodes. The following will be obtained:



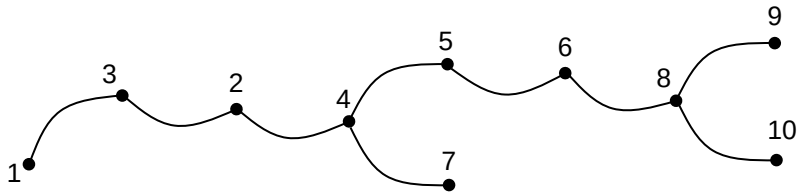
(1,2,3,4,5,6,7,8,9,10)
(3,2,4,4,5,6,7,8)

Continuing this action until deleting all the numbers in the code, this is obtained:



(1,2,3,4,5,6,7,8,9,10)
(3,2,4,4,5,6,7,8)

The last, final step in the connection of not deleted nodes with 8 and 10 numbers in the end.



7b14.

To verify the wholeness of $\left\{x_1^{x_3} v x_2^{x_1}, x_1 \to \bar{x}_2, x_1 \oplus x_2\right\}$ system it is enough to use Post theorem. It is clear that

$x_1 \to \bar{x}_2 \notin T_0$, as $0 \to \bar{0} = 1$;

$x_1 \oplus x_2 \notin T_1$, as $1 \oplus 1 = 0$;

$x_1 \oplus x_2 \notin S$, as the functions depending on two variables are not self-dual;

$x_1 \oplus x_2 \notin M$, as $(0,1) \le (1,1)$ whereas $0 \oplus 1 = 1$, $1 \oplus 1 = 0$;

$x_1 \to \bar{x}_2 \notin L$, as $x_1 \to \bar{x}_2 = \bar{x}_1 \vee \bar{x}_2 = \overline{x_1 x_2} = 1 \oplus x_1 x_2$, i.e. Zhegalkin polynomial contains sum of variables.

Therefore, the system is complete.

7b15.

$\xi_1 = 2$, $\xi_2 = 5$, $\xi_3 = 7$, $\xi_4 = 10$, w=10.

As $\xi_2 + \xi_3 = 5 + 7 = 12 > 10$ ¨ $\xi_4 \ge 10$, the threshold function will be:

$x_2 x_3 \vee x_4$,

x_1 variable's activity of this function equals 0, as x_1 is fictitious variable.

$$\omega_2^{x_2 x_3 \vee x_4} = \left\|\bar{x}_4\right\| \omega_2^{x_2 x_3} = \frac{1}{2} \cdot \left\|x_3\right\| = \frac{1}{2} \cdot \frac{1}{2} = \frac{1}{4}.$$

Due to symmetry

$$\omega_3^{x_2 x_3 \vee x_4} = \frac{1}{4}.$$

$$\omega_4^{x_2 x_3 \vee x_4} = \left\|\overline{x_2 x_3}\right\| \omega_4^{x_4} = 1 - \left\|x_2 x_3\right\| = 1 - \frac{1}{4} = \frac{3}{4}.$$

7b16.

To verify the wholeness of $\left\{x_1 x_2, x_1 \to x_2, x_1 \oplus x_2, x_1 v x_2\right\}$ system it is enough to use Post theorem. It is clear that

$x_1 \to x_2 \notin T_0$, as $0 \to 0 = 1$;

$x_1 \oplus x_2 \notin T_1$, as $1 \oplus 1 = 0$;

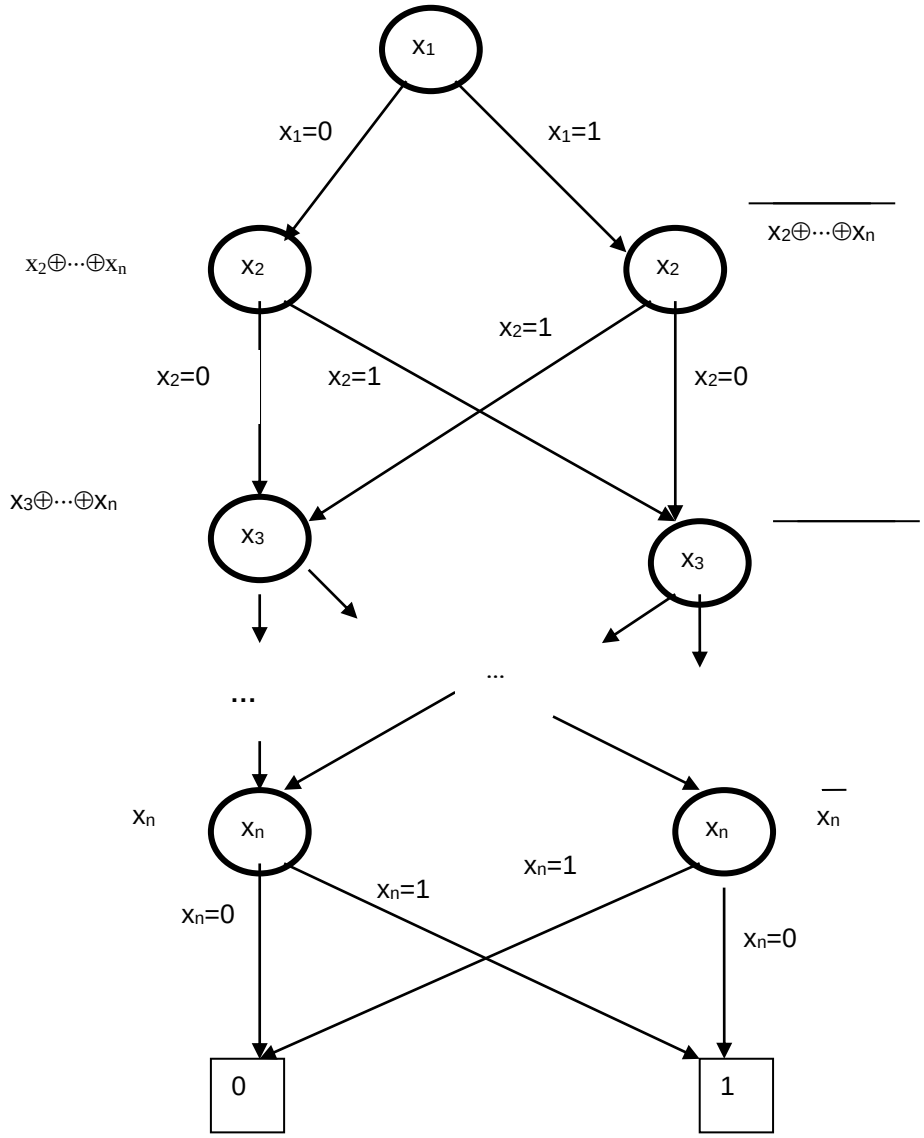
$x_1 \oplus x_2 \notin S$, as $\overline{\bar{x}_1 \oplus \bar{x}_2} = \overline{x_1 \oplus x_2} + x_1 \oplus x_2$;

$x_1 \oplus x_2 \notin M$, as $(0,1) \le (1,1)$ whereas $0 \oplus 1 = 1$, $1 \oplus 1 = 0$;

$x_1 \to \bar{x}_2 \notin L$, as $x_1 \to x_2 \equiv x_1 \oplus x_2 = x_1 x_2$, i.e. Zhegalkin polynomial contains sum of variables.

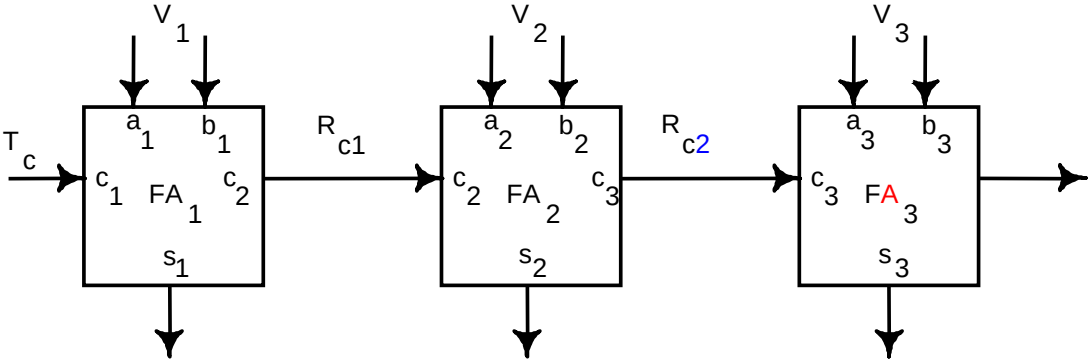
Therefore, the system is complete.

7b17.



7b18.

Figure depicts the corresponding modular form of n-bit adder, as well as the input vectors of the main modules and the corresponding output vectors.



T_c	V_1
0	00
0	01
0	10
0	11
1	00
1	01
1	10
1	11

R_{c1}	V_2
0	00
0	01
0	10
1	00
0	11
1	01
1	10
1	11

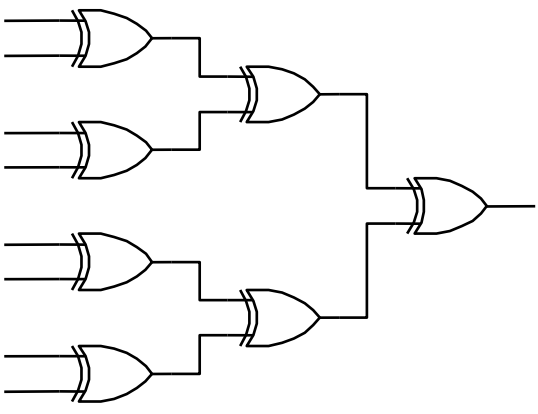
R_{c2}	V_3
0	00
0	01
0	10
0	11
1	00
1	01
1	10
1	11

The input variables for module F_1 are the only variable c_1 of set T_c and the variables a_1, b_1 of set V_1. For modules F2, F3,etc, the input variables are c_2, c_3, etc., of group R_c, as well as the variables a_2, b_2, a_3, b_3, etc., of groups V_2, V_3, etc. The output variable c_{i+1} of module F_i is an input for the input variable c_{i+1} directly connected with the input variable of module F_{i+1}. The variables of groups T_c and V_i are independent, and the variables of groups R_c are dependent (not independent). The variables of groups T_c and R_{c1} accept exhaustively all 8 possible values. The variables of groups R_{ci} and V_{i+1} also accept exhaustively all 8 possible values.

Tc	V1	V2	V3
0	00	00	00
0	01	01	01
0	10	10	10
0	11	00	11
1	00	11	00
1	01	01	01
1	10	10	10
1	11	11	11

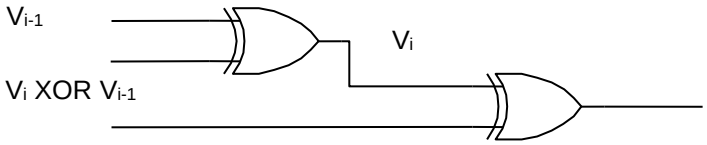
Thus, taking all 8 test vectors depicted in the figure it is possible to provide all 3 inputs for all modules F_i exhaustively all 8 test vectors which will exhaustively detect all possible faults on all input and output lines of module F_i.

7b19.
Figure depicts the corresponding circuit of an N-input parity tree.

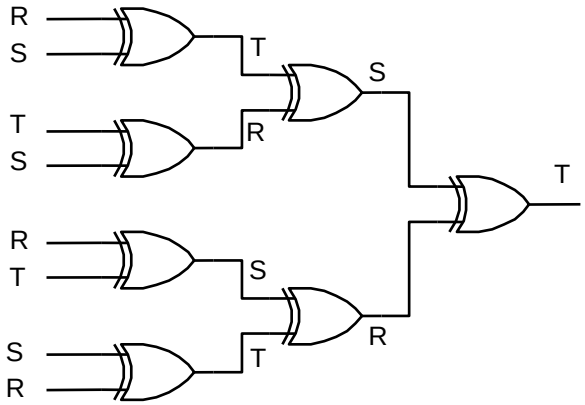


In 1970, Bossen proved that is easily testable by means of only 4 test vectors. By taking the test consisting of 4 exhaustive tests for Modulo 2 logical element (gate XOR): { 00, 01, 10, 11}, and

performing the following assignment for input vectors: R=1100, S=1010, T=0110, and after the following labeling in the parity tree it can be shown that for any V_i, V_j, $V_k \in \{R, S, T\}$, $V_i \neq V_j \neq V_k$ there is $V_i \oplus V_j = V_k$.



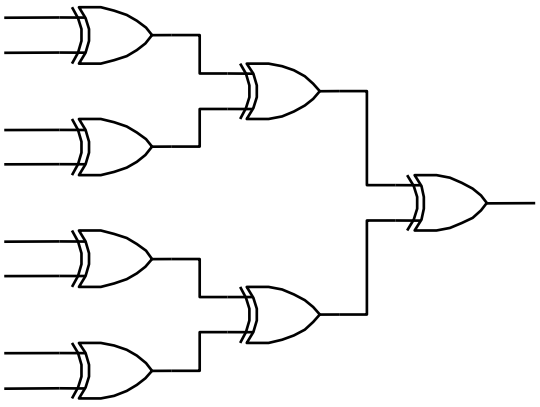
Then performing any labeling in the parity tree of the first figure, the next figure is obtained:



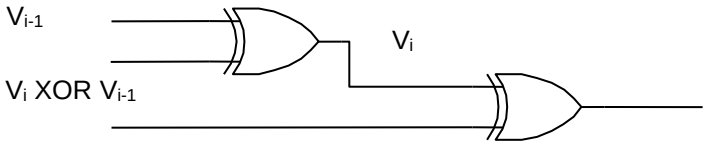
and it is possible to show that the whole parity tree can be tested by means of only 4 test vectors.

Vector	R	S	T	S	R	T	S	R
1	1	1	0	1	1	0	1	1
2	1	0	1	0	1	1	0	1
3	0	1	1	1	0	1	1	0
4	0	0	0	0	0	0	0	0

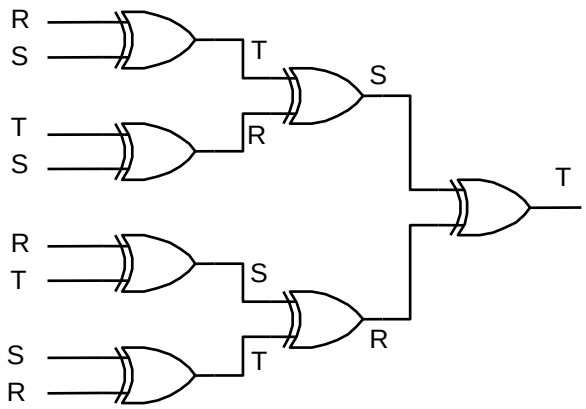
7b20.
Figure depicts the circuit of N-input tree with negated Modulo 2 elements (gates NXOR).



By taking the exhaustive test consisting of 4 vectors for Modulo 2 element (gate NXOR): { 00, 01, 10, 11}, and performing the following assignment for input vectors: R=1010, S=0110, T=0011, and making the following labeling in our tree , the following figure is obtained:



and it is possible to show that for any V_i, V_j, $V_k \in \{R, S, T\}$, $V_i \neq V_j \neq V_k$ there is $V_i \oplus V_j = V_k$. Then by performing any labeling in the tree of Figure 1



It is possible to show that by means of only 4 test vectors the whole tree can be tested.

Vector	R	S	T	S	R	T	S	R
1	1	0	0	0	1	0	0	1
2	0	1	0	1	0	0	1	0
3	1	1	1	1	1	1	1	1
4	0	0	1	0	0	1	0	0

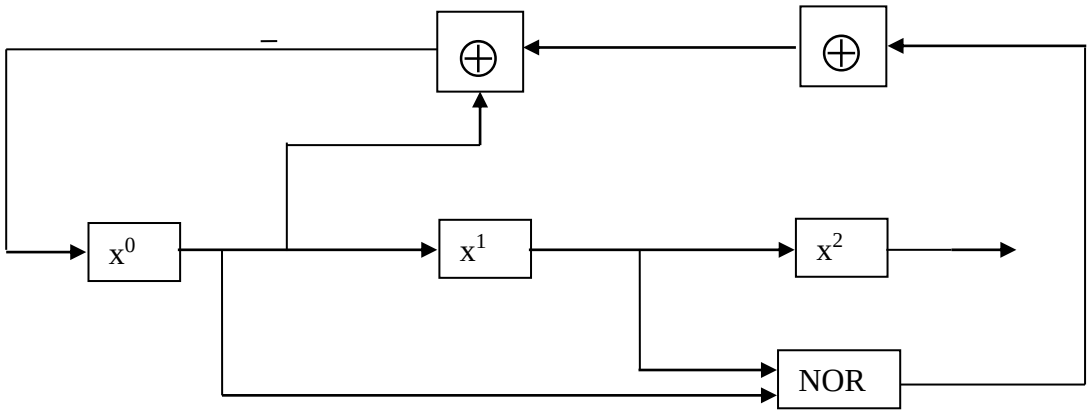
7b21.
The number of all faults is equal

$$\sum_{k=2}^{N} \binom{m}{k} 2^m = 3^N - \binom{N}{0}2^0 - \binom{N}{1}2^1 = 3^N - 2N - 1.$$

Therefore, the number of all stuck-at-0 and stuck-at-1 faults will be
$3^{1000000} - 1999999$.

7b22.
2 subsets are obtained, the corresponding cycles of which include the following sets:
1. (100) => (110) =>(111)=>(011) => (101) =>(010) => (001) => (001)=>(100) ¨
2. (000) =>(000)

7b23.
After adding NOR element, the obtained new circuit generates the only subset of the following patterns:
1. (100) => (110) =>(111)=>(011) => (101) =>(010) => (001) => (001)=>(000) =>(100):



7b24.
First, it is needed to build truth table.

x_1	x_2	x_3	$x_1 \oplus x_3^{x_1 \vee x_2}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Search Zhegalkin polynomial of mentioned function in the following form:

$$f=a_0 \oplus a_1x_1 \oplus a_2x_2 \oplus a_3x_3 \oplus a_{12}x_1x_2 \oplus a_{13}x_1x_3 \oplus a_{23}x_2x_3 \oplus a_{123}x_1x_2x_3$$

The solution of the problem is to find coefficients in the presented form.
Function is equal 1 with values 0,0,0 of arguments x1, x2, x3 . Placing these values on right side of equation:

$1= a_0$

For values 0,0,1 it will be
$0=1 \oplus a_3$ therefore: $a_3=1$:

Substituting the right and left parts of the equation, sequentially all the possible values to x_1, x_2 and x_3 variables, the following will be obtained:

$0 = 1 \oplus a_2$, $a_2 = 1$,
$1 = 1 \oplus 1 \oplus 1 \oplus a_{23}$, $a_{23} = 0$,
$1 = 1 \oplus a_1$, $a_1 = 0$,
$0 = 1 \oplus 1 \oplus a_{13}$, $a_{13} = 1$,
$1 = 1 \oplus 1 \oplus a_{12}$, $a_{12} = 1$'
$0 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus a_{23}$, $a_{23} = 0$,

Putting the obtained values of the coefficients, Zhegalkin polynomial of the function will be obtained.

$$f=1 \oplus x_2 \oplus x_3 \oplus x_1x_2 \oplus x_1x_3 \oplus x_1x_2x_3$$

7b25.
There is some tree corresponding to 000101001111, mark it using the folowing symbol:

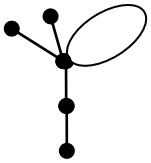
As code cannot be divided into 2 parts, each containing equal number of 1s and 0s, the tree will have the following view:

the ring code of which is 0010100111, which is derived from base code by removing 0 and 1 from each side.

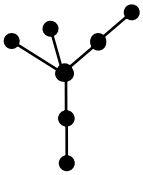
Repeating this procedure to new code, the following will be obtained respectively:

 and 01010011:

On next step code is divided to 01, 01 ¨ 0011 parts and this will be obtained:



On last step, as 0011 cannot be divided into 2 parts, this will be obtained:



7b26.

$$\omega_1^{x_1x_2\oplus(x_1\vee x_2x_3)} = \|x_2x_3 \oplus (x_2 \oplus 1)\| = \|x_2x_3 \oplus \bar{x}_2\| = \|x_2x_3\| + \|\bar{x}_2\| = \frac{1}{4} + \frac{1}{2} = \frac{3}{4}$$

$$\omega_2^{x_1x_2\oplus(x_1\vee x_2x_3)} = \|x_1 \oplus (x_1 \oplus (x_1 \vee x_3))\| = \|x_1 \oplus x_1 \oplus (x_1 \vee x_3)\| = \|x_1 \vee x_3\| = \frac{1}{2} + \frac{1}{2} - \frac{1}{4} = \frac{3}{4}$$

$$\omega_3^{x_1x_2\oplus(x_1\vee x_2x_3)} = \|(x_1x_2 \oplus x_1) \oplus (x_1x_2 \oplus (x_1 \vee x_2))\| = \|(x_1x_2 \oplus x_1 \oplus x_1x_2 \oplus (x_1 \vee x_2))\| =$$

$$= \|(x_1 \oplus (x_1 \vee x_2))\| = \frac{1}{2} + \frac{3}{4} - 2\|(x_1 \oplus (x_1 \vee x_2))\| = \frac{1}{2} + \frac{3}{4} - 1 = \frac{1}{4}$$

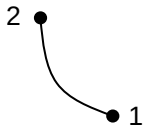
7b27.

As the code length equals 7, therefore the number of tree nodes equals 9. The numbers of those nodes and tree code are:

1, 2, 3, 4, 5, 6, 7, 8, 9:

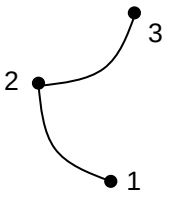
From those numbers choose the number from left to right which is missing in the code. It is 1. Connect the node of that number with number one node of the code from the left (which is 2) and delete those two numbers. The following will be obtained:

3, 3, 4, 5, 5, 8
2, 3, 4, 5, 6, 7, 8, 9:



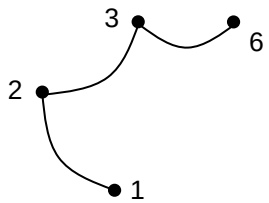
Apply the same process sequentially towards the obtained results, connect the node of 3 number with the node 3. The following will be obtained:

3, 4, 5, 5, 8
3, 4, 5, 6, 7, 8, 9

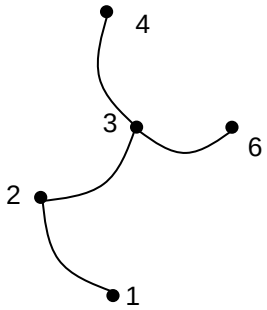


Continuing this action until deleting all the numbers in the code, this is sequentially obtained:

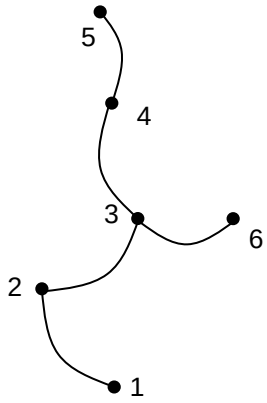
4, 5, 5, 8
3, 4, 5, 7, 8, 9



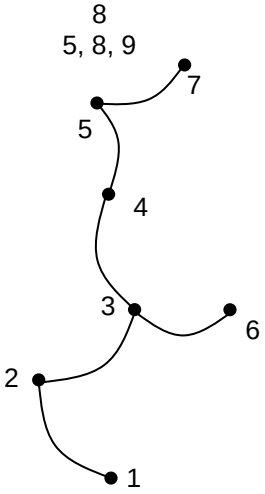
5, 5, 8
4, 5, 7, 8, 9

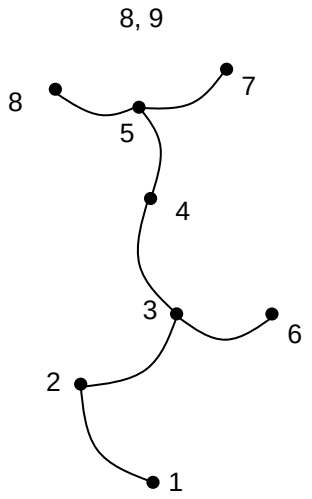


5, 8
5, 7, 8, 9

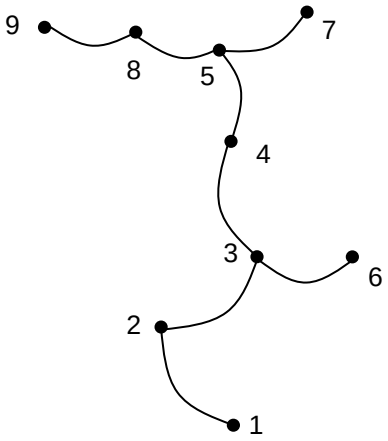


8
5, 8, 9





Finally remaining 8 and 9 nodes are connected to each other.



8. OBJECT-ORIENTED PROGRAMMING

a) Test questions

8a1. B
8a2. B
8a3. E
8a4. D
8a5. B
8a6. C
8a7. A
8a8. B
8a9. C
8a10. D
8a11. B
8a12. D
8a13. C
8a14. A
8a15. A
8a16. C
8a17. E
8a18. E
8a19. C
8a20. A
8a21. D
8a22. B
8a23. E
8a24. E
8a25. C
8a26. D
8a27. C
8a28. C
8a29. E
8a30. B
8a31. E
8a32. D
8a33. B
8a34. A
8a35. B
8a36. A
8a37. B
8a38. A
8a39. B
8a40. E
8a41. E
8a42. C
8a43. B
8a44. D
8a45. D
8a46. D
8a47. C
8a48. E
8a49. D
8a50. B
8a51. D

b) Problems

8b1.

Length of the greatest common subsequence can be computed using the following program:

```
#include <stdio.h>
#define N 1000
#define max(a,b) ((a>b) ? a : b)
int L[N][N];
int main()
{
    char a[N];
    char b[N];
    int i, j, n, m;
    int yes = 0;
    scanf("%s", a);
    scanf("%s", b);
    n = strlen(a);
    m = strlen(b);
    for( j = 0; j < m ; j++ )
    {
       if( b[j] == a[0] ) yes = 1;
       L[0][j] = yes;
    }
    yes = 0;
    for(i = 0; i < n; i++)
    {
       if( a[i] == b[0] ) yes = 1;
       L[i][0] = yes;
    }
    for(i = 1; i < n; i++)
    {
       for(j = 1; j < m ; j++)
       {
             if( a[i] == b[j] )
             L[i][j] = L[i-1][j-1] + 1;
```

```
          else
             L[i][j] = max( L[i-1][j], L[i][j-1] );
       }
    }
    printf( "%d\n",  L[n-1][m-1] );
    return 0;
}
```

8b2.
AM(10,10)= 7368

8b3.
Sum of digits =150
Q=3.752002426043100302699428993946639820.

8b4.
```
Subs(n,k):=
  If (n==k) then Ss={{1,2,3,...,n}};
                    goto END;
               else A={1,...,k}
  end;
  Ss={};
  p=k;
  label P
  Ss=Ss⊕A;
  If (A(k)==n) then p=p-1
                 else p=k
  end;
  If (p>=1) then i=k+1;
                  label Q;
                  i-i-1;
                  If(i>=p) then A(i)=A(p)+i-p+1;
                                  goto Q
                            else goto P;
                  end;
  end;
label END;
Rerurn(Ss)
```

8b5.
Use Induction. The loop invariant is the following: $x_j y_j^{z_j} = y_0^{z_0}$

8b6.
Use Induction.

8b7.
Use Induction.

8b8.
```
#include <iostream>

using namespace std;

int main()
{
       int n;
       cin >> n;
       cout << n - (n/2 + n/3 + n/5 - n/6 - n/15 - n/10 + n/30) << endl;
       return 0;
}
```

8b9.

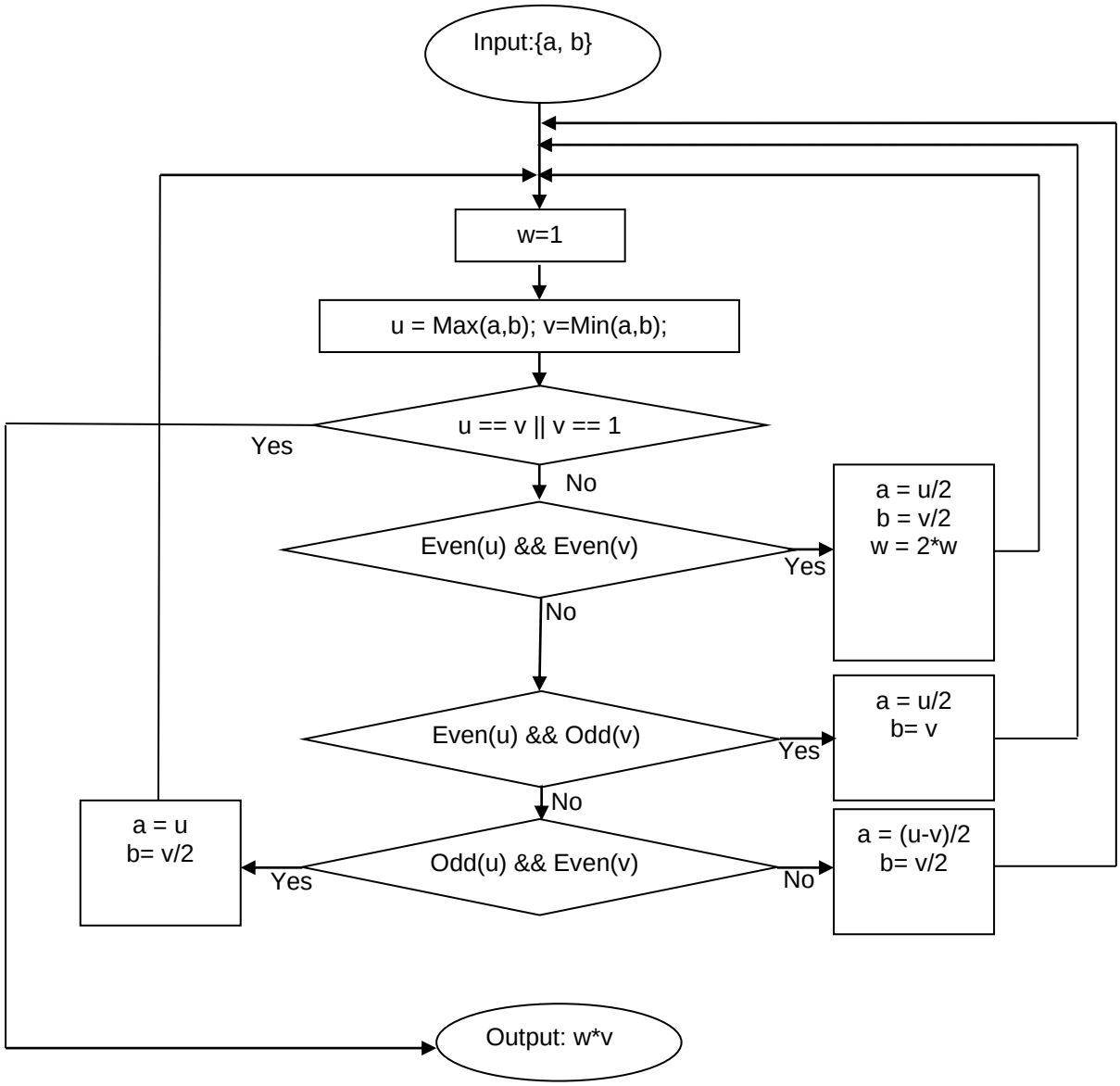
```
#include <iostream>
#include <fstream>
#include <cmath>
#include <algorithm>
#include <set>
#include <queue>
#include <stack>
#include <iomanip>

using namespace std;

struct matric
{
	int a[2][2];
};

matric a1;

matric mul(matric a,matric b)
{
	int i,j,k;
	matric h;
	for (i=0;i<2;i++)
		for (j=0;j<2;j++)
			h.a[i][j]=0;
	for (i=0;i<2;i++)
		for (j=0;j<2;j++)
			for (k=0;k<2;k++)
			{
				h.a[i][j]= ((__int64)h.a[i][j] +
(__int64)a.a[i][k]*b.a[k][j]) % 1000007;
				h.a[i][j]%=1000007;
			}
	return h;
}

matric stepen(matric a,int n)
{
	if (n==1)
		return a;
	matric h=stepen(a,n/2);
	h=mul(h,h);
	if (n&1)
		h=mul(h,a1);
	return h;
}


int main()
{
	int n;

	cin >> n;

	a1.a[0][0]=1;a1.a[0][1]=1;
	a1.a[1][0]=1;a1.a[1][1]=0;

	matric h1 = stepen(a1,n);

	cout << h1.a[0][0] << endl;

	return 0;
}
```

8b10.

```
#include <iostream>
#include <fstream>
```

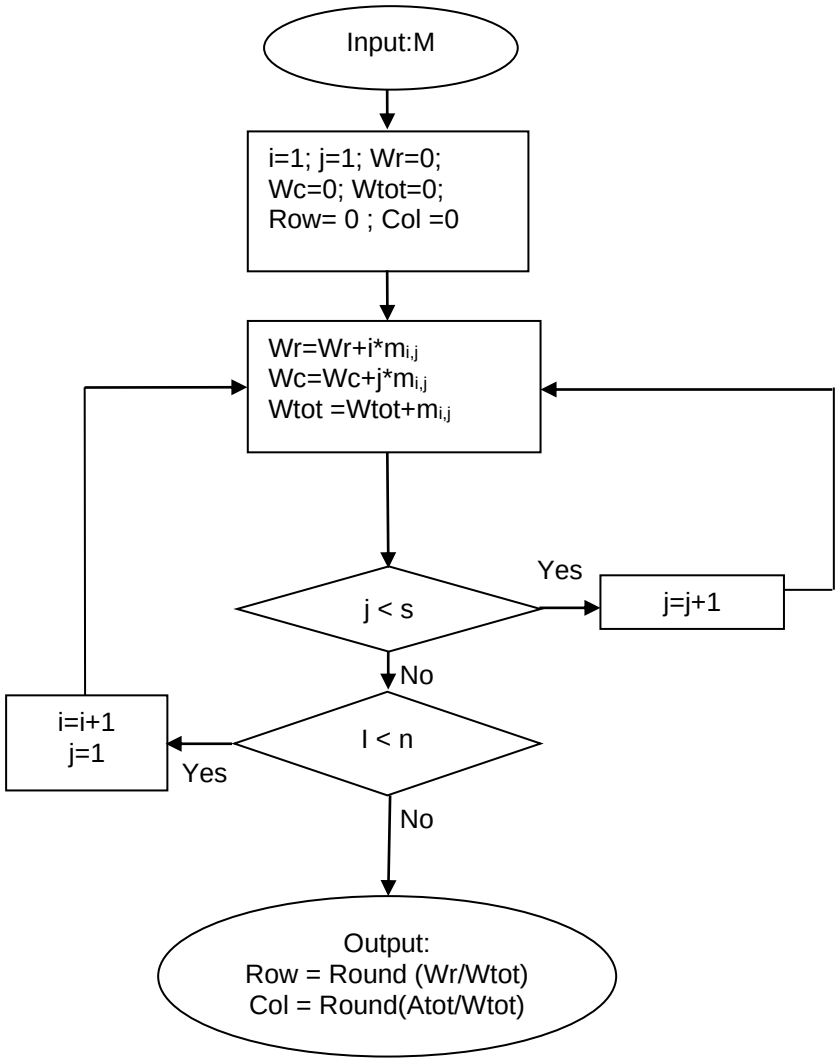
```
using namespace std;

ifstream in("15.in");
ofstream out("15.out");
int number,arr[5000],ans[5000];
int i,j,max;
int main()
{
	in >> number;
	for (i=0;i<number;i++)
		in >> arr[i];
	for (i=0;i<number;i++)
	{
		max=0;
		for (j=0;j<i;j++)
			if (arr[j]<arr[i] && max<ans[j])
				max=ans[j];
		ans[i]=max+1;
	}
	max=0;
	for (i=0;i<number;i++)
		if (ans[i]>max)
			max=ans[i];
	out << max << endl;
	return 0;
}
```

8b11.
We assume that detection Odd/Even as well as division of even integers by 2 are operations that are to be made with the last position of binary representations and hence do not use the deletion in common sense.



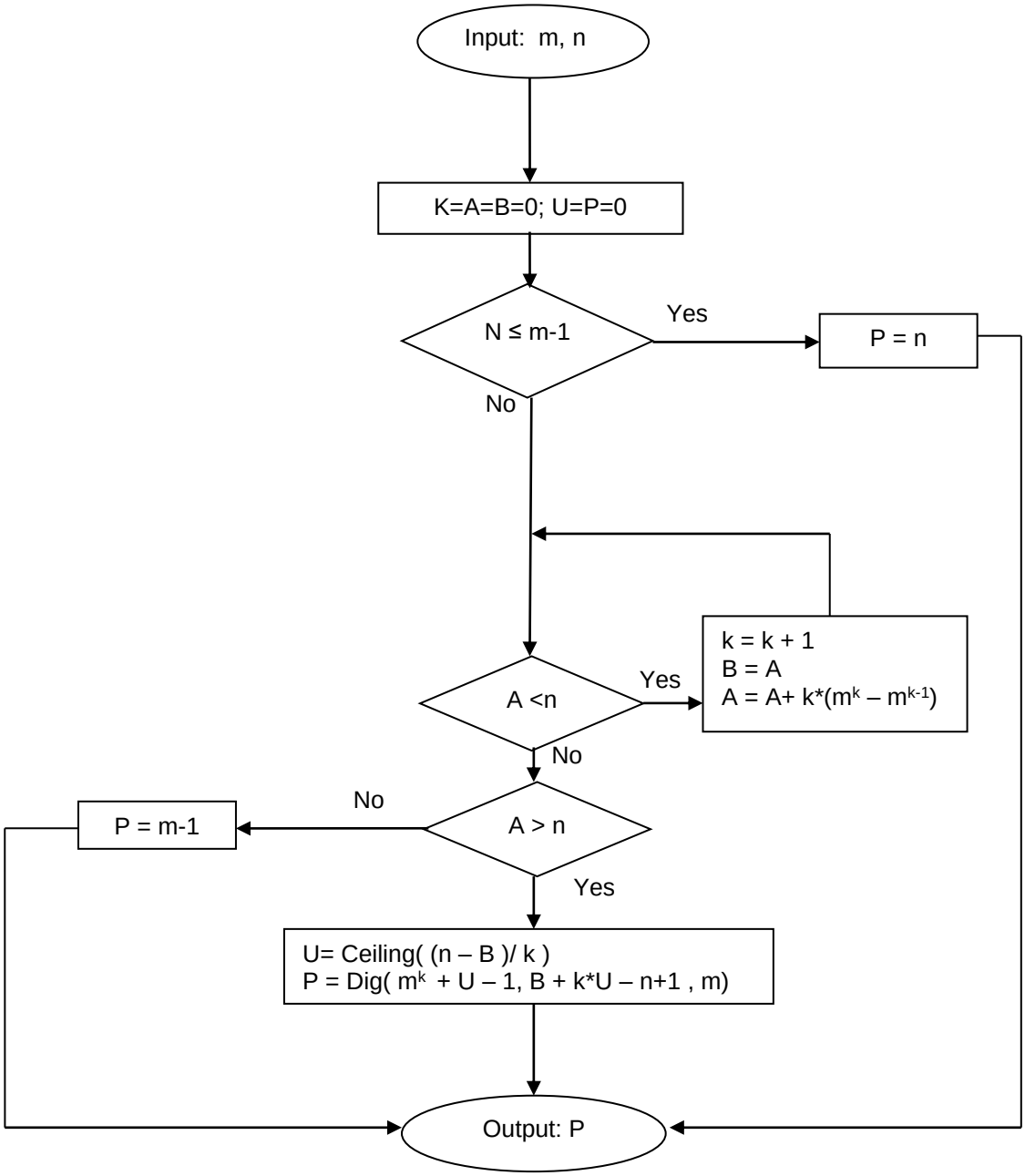
8b12.

A.

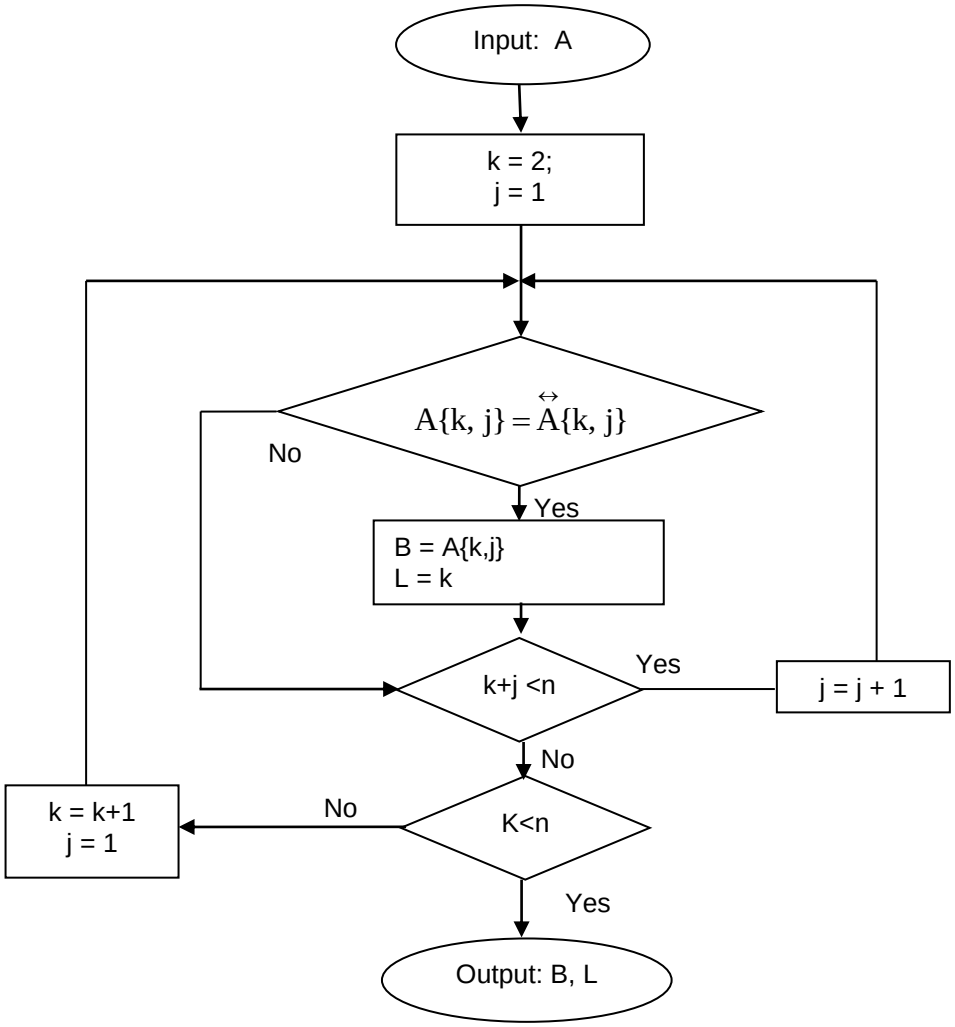

Input:M
i=1; j=1; Wr=0;
Wc=0; Wtot=0;
Row= 0 ; Col =0
Wr=Wr+i*m_{i,j}
Wc=Wc+j*m_{i,j}
Wtot =Wtot+m_{i,j}
j < s
Yes
j=j+1
No
I < n
i=i+1
j=1
Yes
No
Output:
Row = Round (Wr/Wtot)
Col = Round(Atot/Wtot)

B. O(n*s).

8b13.
Dig(x,y,z) = Mod(Floor(x/z^{y-1}), z), i.e Dig(x,y,z) is equal to y-th digit (from the right side) in z-ary representation of the number x.



8b14.



Here $A\{k, j\}$ denotes a fragment of A having length k and startpoint j, and $\overleftrightarrow{A}\{k, j\}$ denotes the reflection (in miror) of $A\{k, j\}$.

8b15.

```
#include <iostream>
#include <cmath>

int main()
{
    const int n = 1000;
    const int size = 200;
    int prime_numbers[size] = {0};
    int index = 0;

    for (int i = 2; i <= n; ++i) {
        int limit = (int)sqrt(i);
        int j = 2;
        for (; j <= limit; ++j) {
            if (0 == i % j) {
                break;
            }
        }
        if (j > limit) {
```

```
            prime_numbers[index] = i;
            ++index;
        }
    }

    for (int k = 0; k < index; ++k) {
        std::cout << prime_numbers[k] << " ";
    }
    std::cout << std::endl;

    return 0;
}
```

8b16.

```
#include <iostream>

int main()
{
    const int n = 1000;
    const int size = 20;
    int perfect_numbers[size];
    int index = 0;

    for (int i = 2; i <= n; ++i) {
        int sum = 0;
        int limit = i/2;
        for (int j = 1; j <= limit; ++j) {
            if (0 == i % j) {
                sum += j;
            }
        }
        if (i == sum) {
            perfect_numbers[index] = i;
            ++index;
        }
    }

    for (int k = 0; k < index; ++k) {
        std::cout << perfect_numbers[k] << " ";
    }
    std::cout << std::endl;

    return 0;
}
```

8b17.

```
#include <iostream>

long reverse_number(long n);

int main()
{
    std::cout << "Please enter the number: ";
    long n;
    std::cin >> n;
    long reverse_n = reverse_number(n);
    if (n == reverse_n) {
        std::cout << "Yes"  << std::endl;
    } else {
        std::cout << "No" << std::endl;
    }

    return 0;
}
```

```
long reverse_number(long n)
{
    long reverse = 0;
    do  {
        reverse = reverse * 10 + n % 10;
        n /= 10;
    } while (n != 0);

    return reverse;
}
```

A BOOK OF TESTS AND PROBLEMS OF THE ARMENIAN MICROELECTRONICS OLYMPIADS

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